MegaCore IP Library

Release Notes and Errata

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Feedback

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About These Release Notes

These release notes cover versions 11.0 through 12.0 of the Altera® MegaCore® IP Library. The chapters in these release notes describe the revision history and errata for each product in the MegaCore IP Library.

From v8.0 onwards, this document replaces all individual IP product release notes and errata sheets that Altera previously published.

From v11.1 onwards, for full information on errata and the versions affected by errata, refer to the Knowledge Base page of the Altera website.

Errata are functional defects or errors, which may cause the product to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

For more information about Quartus® II issues, refer to the Knowledge Base page of the Altera website.

Trademarks

These release notes use the following Altera trademarks:

- Arria® devices
- Avalon® interface
- Cyclone® devices
- HardCopy® devices
- MegaCore function
- MegaWizard™ Plug-In
- ModelSim® simulator
- Nios® II processor
- Quartus II software
- SignalTap® II logic analyzer
- Stratix® devices

System Requirements

The MegaCore IP Library is distributed with the Quartus II software and downloadable from the Altera website, www.altera.com.

For system requirements and installation instructions, refer to Altera Software Installation and Licensing.

Chapter Revision Dates

The chapters in this document, MegaCore IP Library, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. 8B10B Encoder/Decoder
Revised: *1 July 2012*
Part Number:

Chapter 2. 10GBASE-R PHY
Revised: *1 July 2012*
Part Number:

Chapter 3. 10-Gbps Ethernet MAC
Revised: *1 July 2012*
Part Number:

Chapter 4. 40- and 100-Gbps Ethernet MAC and PHY
Revised: *1 July 2012*
Part Number:

Chapter 5. Arria V Hard IP for PCI Express
Revised: *1 July 2012*
Part Number:

Chapter 6. ASI
Revised: *1 July 2012*
Part Number:

Chapter 7. CIC
Revised: *1 July 2012*
Part Number:

Chapter 8. CPRI
Revised: *1 July 2012*
Part Number:

Chapter 9. CRC Compiler
Revised: *1 July 2012*
Part Number:

Chapter 10. Cyclone V Hard IP for PCI Express
Revised: *1 July 2012*
Part Number:

Chapter 11. DDR and DDR2 SDRAM Controller Compiler
Revised: *1 July 2012*
Part Number:

Chapter 12. DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP
Revised: *1 July 2012*
Part Number:

Chapter 13. DDR3 SDRAM Controller with ALTMEMPHY IP
Revised: *1 July 2012*
Part Number:

Chapter 14. DDR2, DDR3, and LPDDR2 SDRAM Controller with UniPHY
Revised: *1 July 2012*
Part Number:

Chapter 15. FFT
Revised: *1 July 2012*
Part Number:

Chapter 16. FIR Compiler
Revised: *1 July 2012*
Part Number:

Chapter 17. FIR Compiler II
Revised: *1 July 2012*
Part Number:

Chapter 18. Interlaken
Revised: *1 July 2012*
Part Number:

Chapter 19. Interlaken PHY
Revised: *1 July 2012*
Part Number:

Chapter 20. IP Compiler for PCI Express
Revised: *1 July 2012*
Part Number:

Chapter 21. NCO
Revised: *1 July 2012*
Part Number:

Chapter 22. Nios II Processor
Revised: *1 July 2012*
Part Number:

Chapter 23. PCI Compiler
Revised: *1 July 2012*
Part Number:

Chapter 24. POS-PHY Level 4
Revised: *1 July 2012*
Part Number:

Chapter 25. QDRII SRAM
Revised: *1 July 2012*
Part Number:

Chapter 26. QDR II and QDR II+ SRAM Controller with UniPHY
Revised: *1 July 2012*

Part Number:

Chapter 27. RapidIO
Revised: *1 July 2012*
Part Number:

Chapter 28. Reed-Solomon Compiler
Revised: *1 July 2012*
Part Number:

Chapter 29. Reed-Solomon II
Revised: *1 July 2012*
Part Number:

Chapter 30. RLDRAM II
Revised: *1 July 2012*
Part Number:

Chapter 31. RLDRAM II Controller with UniPHY
Revised: *1 July 2012*
Part Number:

Chapter 32. SDI
Revised: *1 July 2012*
Part Number:

Chapter 33. SerialLite II
Revised: *1 July 2012*
Part Number:

Chapter 34. Stratix V Hard IP for PCI Express
Revised: *1 July 2012*
Part Number:

Chapter 35. Triple Speed Ethernet
Revised: *1 July 2012*
Part Number:

Chapter 36. Video and Image Processing Suite
Revised: *1 July 2012*
Part Number:

Chapter 37. Viterbi Compiler
Revised: *1 July 2012*
Part Number:

Chapter 38. XAUI PHY
Revised: *1 July 2012*
Part Number:

1. 8B10B Encoder/Decoder

Product Revision History

Table 1–1 shows the revision history for the 8B10B Encoder/Decoder MegaCore function.

For more information about the new features, refer to the *8B10B Encoder/Decoder MegaCore Function User Guide*.

Table 1–1. 8B10B Encoder/Decoder MegaCore Function Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	Maintenance release.
11.0	May 2011	Final support for Arria II GX, Stratix IV GX, Cyclone III LS, Cyclone IV GX, and Cyclone IV E devices.

Errata

No known issues in v11.1, v11.0, and v10.1.

Product Revision History

Table 2–1 shows the revision history for the 10GBASE-R PHY IP core.

For more information about the new features, refer to the "10GBASE-R PHY IP Core" chapter in the *Altera Transceiver PHY IP Core User Guide*.

Table 2–1. 10GBASE-R PHY Revision History

Version	Data	Description
12.0	June 2012	■ Added Arria V device support. ■ Added the following QSF settings to all transceiver PHY: ■ XCVR_TX_PRE_EMP_PRE_TAP_USER ■ XCVR_TX_PRE_EMP_2ND_POST_TAP_USER ■ Added 11 new settings for GT transceivers. ■ Added optional pll_locked status signal for Arria V and Stratix V devices. ■ Added optional rx_coreclkin port.
11.1 SP2	February 2012	Verified with the Quartus II software v11.1 SP2.
11.1 SP1	December 2011	Verified with the Quartus II software v11.1 SP1.
11.1	November 2011	Added support for Stratix V devices.
11.0	May 2011	Verified with the Quartus II software v11.0.

Errata

For a recent list of errata and affected versions of the 10GBASE-R PHY IP Core IP core, refer to the Altera Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other critera.

Not all issues affect all versions of the 10GBASE-R PHY IP Core.

Table 2–2 lists the errata for the 10GBASE-R PHY IP Core, the relevant software releases, and links to the Knowledge Base.

Table 2–2. 10GBASE-R PHY IP Core Errata Knowledge Base Links

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
rx_oc_busy Port Is Not A Top-Level Signal	8-Feb-12	Version 11.0	Version 11.1 SP2	http://www.altera.com/support/kdb/solutions/spr317295.html
Mixed Language Simulation Fails when Optimization Is On	16-Sep-11	Version 10.1	Version 11.1	http://www.altera.com/support/kdb/solutions/spr357410.html
Simulation of 10GBASE-R, Custom, Interlaken, Low Latency, PCI Express PIPE, and XAUI Transceiver PHY IP Cores Fails for Stratix V if You Use ModelSim With Mixed Languages	11-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr362110.html

Product Revision History

Table 3–1 shows the revision history for the 10-Gbps Ethernet (10GbE) MAC MegaCore function.

For more information about the new features, refer to the *10-Gbps Ethernet MAC MegaCore Function User Guide.*

Table 3–1. 10-Gbps Ethernet MAC MegaCore Function Revision History

Version	Date	Description
12.0	July 2012	Preliminary support for Arria V GT devices.
11.1	November 2011	Maintenance release.
11.0	May 2011	■ Final support for Cyclone IV GX, Arria II GZ and HardCopy IV GX devices. ■ Added preamble passthrough mode, datapath option, and PFC features.

Errata

For the most recent list of errata for the 10-Gbps Ethernet (10GbE) MAC MegaCore function, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the Video and Image Processing Suite MegaCore functions.

Table 3–2 lists the errata for the 10GbE MAC MegaCore function, the relevant software releases, and links to the Knowledge Base.

Table 3–2. 10GbE MAC MegaCore Function Errata Knowledge Base Links (Part 1 of 2)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
Data Transmission Not Resumed Immediately When 10GbE MAC Receives PFC Frame	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr378245.html
Missing FCS Field in Flow Control Frame	15-Feb-12	Version 11.0		http://www.altera.com/support/kdb/solutions/fb35672.html
Empty Source Address Field in Flow Control Frame	15-Feb-12	Version 11.0		http://www.altera.com/support/kdb/solutions/fb35671.html
Error When Generating Simulation Model Using MegaWizard Plug-in Manager	13-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr377724.html

Table 3–2. 10GbE MAC MegaCore Function Errata Knowledge Base Links (Part 2 of 2)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
64-bit ModelSim Simulator Fails to Simulate 10GbE MAC with XAUI PHY Design Example	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr370793.html
Recovery Failure for 10GbE MAC with 10GBASE-R PHY Design Example in Stratix IV Devices	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr374663.html
Simulation Not Supported for Stratix V Designs	15-Nov-11	Version 10.0	Version 11.0	http://www.altera.com/support/kdb/solutions/spr392686.html
Simulation Not Supported for Stratix V Designs	15-Nov-11	Version 10.0	Version 11.0	http://www.altera.com/support/kdb/solutions/spr342892.html
TimeQuest Timing Analyzer Failure for 10GbE MAC with 10GBASE-R PHY Design Example in Stratix V Devices	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr374494.html
No Length Checking for VLAN and Stacked VLAN Frames	15-Nov-11	Version 10.0	Version 11.0	http://www.altera.com/support/kdb/solutions/spr342891.html

4. 40- and 100-Gbps Ethernet MAC and PHY

Product Revision History

Table 4–1 shows the revision history for the 40- and 100-Gbps Ethernet MAC and PHY.

For more information about the new features, refer to the *40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide*.

Table 4–1. 40- and 100-Gbps Ethernet MAC and PHY Revision History

Date	Version	Description
June 2012	12.0	First release.

Errata

For the most recent list of errata for the 40- and 100-Gbps Ethernet MAC and PHY MegaCore function, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Table 4–2 lists the errata for the 40- and 100-Gbps Ethernet MAC and PHY MegaCore function, the relevant software versions, and the links to the Knowledge Base.

Table 4–2. 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function Errata Knowledge Base Links

Problem	Published Date	Version Found In	Version Fixed In	Knowledge Base Link
Quartus II Fitter Generates 0 ppm Critical Warnings When Regenerating Underlying PHY IP Cores in 40GbE and 100GbE MAC and PHY IP Cores	8-Jun-12	12.0		http://www.altera.com/support/kdb/solutions/fb56713.html
In the 40GbE and 100GbE MAC and PHY IP Core, the Stratix V RX-Only Configuration Shows Bit Errors on Hardware	12-Jun-12	12.0		http://www.altera.com/support/kdb/solutions/fb57785.html
In the 40GbE MAC and PHY IP Core, Critical Warnings are Generated when Compiling Stratix IV Device Designs	12-Jun-12	12.0		http://www.altera.com/support/kdb/solutions/fb57759.html
In 40GbE and 100GbE MAC and PHY IP Cores, the Quartus II Software Reports Minimum Pulse Width Violations for Some 10-Gbps PHY Clock Signals	8-Jun-12	12.0		http://www.altera.com/support/kdb/solutions/fb55569.html
Regenerating Underlying PHY IP Cores in 40GbE and 100GbE MAC and PHY IP Cores	8-Jun-12	12.0		http://www.altera.com/support/kdb/solutions/fb56515.html

Table 4–2. 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function Errata Knowledge Base Links

Problem	Published Date	Version Found In	Version Fixed In	Knowledge Base Link
Meeting timing for Stratix IV devices with the 100GbE MAC and PHY IP Core	8-Jun-12	12.0		http://www.altera.com/support/kdb/solutions/fb57675.html
In the 40GbE and 100GbE MAC and PHY IP core, no top-level wrapper files are provided for the 40GbE and 100GbE MAC IP Cores with adapters	8-Jun-12	12.0		http://www.altera.com/support/kdb/solutions/fb56144.html

5. Arria V Hard IP for PCI Express

Product Revision History

Table 5–1 shows the revision history for the Arria V Hard IP for PCI Express.

For more information about the new features, refer to the *Arria V Hard IP for PCI Express User Guide*.

Table 5–1. Stratix V Hard IP for PCI Express Revision History

Date	Version	Description
June 2012	12.0	■ Added ×1, ×4, and ×8 Gen1 support for Endpoints using the Avalon-MM interface ■ Added ×1 and ×4 Gen2 support for Endpoints using the Avalon-MM interface ■ Added support for dynamic reconfiguration of transceiver settings ■ Added support for VHDL simulation
February 2012	11.1 SP2	Verified with the Quartus II software v11.1 SP2.
December 2011	11.1 SP1	Verified with the Quartus II software v11.1 SP1.
November 2011	11.1	First release.

Errata

For a recent list of errata and affected versions of the Stratix V Hard IP for PCI Express IP core, refer to the Altera Knowledge Base web page.

Not all issues affect all versions of the Arria V Hard IP for PCI Express.

Table 5–2 lists the errata for the Hard IP for PCI Express, the relevant software releases, and links to the Knowledge Base.

Table 5–2. Hard IP for PCI Express Errata Knowledge Base Links (Part 1 of 2)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Arria V Hard IP for PCI Express IP Core V_{OD} Too Low	28-Feb-11	Version 11.1 SP2	Version 12.0	http://www.altera.com/support/kdb/solutions/fb40177.html
PCI Express VHDL Example Design Simulation Fails	8-Feb-12	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr393995.html
Reconfiguration Ports Not Available for Arria V and Cyclone V Hard IP for PCI Express IP Cores	23-Jan-12	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/fb34064.html

Table 5–2. Hard IP for PCI Express Errata Knowledge Base Links (Part 2 of 2)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Downstream Memory Reads (MRds) Fail for Arria V Hard IP for PCI Express	20-Jan-12	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr394004.html
The User Guides for PCI Express Do Not Document How a Variant Handles the Address Translation and Reserved Bits of a TLP Header	17-Nov-11	Version 11.0	Version 12.0	http://www.altera.com/support/kdb/solutions/spr385731.html
Hard IP for PCI Express User Guides Shows Incorrect Value for Receiver Detect Capacitor	03-July-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb61601.html
Arria V and Cyclone V Hard IP for PCI Express IP Cores Do Not Downtrain to x1	13-June-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb57305.html
Multi-Function Parameter Is Incorrectly Set in Arria V and Cyclone V Hard IP for PCI Express IP Cores	08-June-12	Version 11.1		thttp://www.altera.com/support/kdb/solutions/fb54277.html
Arria V Hard IP for PCI Express Should Return an Error When You Select the 64-Bit Interface for Gen1 x8 or Gen2 x4 Variants	20-Dec-11	Version 11.1	Version 11.1 SP2	http://www.altera.com/support/kdb/solutions/spr393333.html
VHDL Compilation Fails for Arria V and Cyclone V Hard IP for PCI Express	8-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr390424.html
Advanced Error Reporting (AER) and ECRC Not Available for Arria V and Cyclone V Hard IP for PCI Express	9-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr392030.html

Product Revision History

Table 6–1 shows the revision history for the ASI MegaCore function.

For more information about the new features, refer to the *ASI MegaCore Function User Guide*.

Table 6–1. ASI MegaCore Function Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	Maintenance release.
11.0	May 2011	Final support for Arria II GZ, Cyclone III LS, and Cyclone IV GX devices.

Errata

For the most recent list of errata for the ASI MegaCore function, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the ASI MegaCore function.

Product Revision History

Table 7–1 shows the revision history for the CIC MegaCore function.

For information about the new features, refer to the *CIC MegaCore Function User Guide*.

Table 7–1. CIC MegaCore Function Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	Maintenance release.
11.0	May 2011	■ Final support for Arria II GX, Arria II GZ, Cyclone III LS, and Cyclone IV GX devices. ■ HardCopy Compilation support for HardCopy III, HardCopy IV E, and HardCopy IV GX devices.

Errata

For the most recent list of errata for the CIC MegaCore function, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Product Revision History

Table 8–1 shows the revision history for the CPRI MegaCore function.

For information about the new features, refer to the *CPRI MegaCore Function User Guide*.

Table 8–1. CPRI MegaCore Function Revision History

Version	Date	Description
12.0	June 2012	■ Added CPRI line rate of 9.8304 Gbps in Arria V GT and Stratix V devices. ■ Added support for autorate negotiation up to 6.144 Gbps in Arria V devices. ■ Added support for autorate negotiation up to 9.8 Gbps in Stratix V devices. ■ Added new parameter to specify inclusion or exclusion of an HDLC block. ■ Added new parameter to specify the MAP interface mapping mode.
11.1 SP2	February 2012	Maintenance release.
11.1 SP1	December 2011	Maintenance release.
11.1	November 2011	■ Added support for Arria V and Stratix V devices. ■ Added Tx elastic buffer and Tx extended delay measurement information. ■ Added new delay measurement features Tx bitslip and autocalibration to enhance the consistency of the round-trip delay through a CPRI RE slave. Support includes two new registers. ■ Added new advanced Method 1 mapping mode and modified the `map_mode` encodings. ■ Added new parameter to enable clocking AxC interfaces with `cpri_clkout`.
11.0	May 2011	■ Upgraded to final support for Arria II GZ and Cyclone IV GX devices. ■ Upgraded to HardCopy Compilation support for HardCopy IV GX devices. ■ Added byte-enable signal. ■ Added parameter to control WIDTH_RX_BUF.

Errata

For the most recent list of errata for the CPRI MegaCore function, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the CPRI MegaCore function. Altera recommends upgrading to the latest available version of the MegaCore IP Library.

Table 8–2 lists the errata for the CPRI MegaCore function, the relevant software versions, and the links to the Knowledge Base.

Table 8–2. CPRI MegaCore Function Errata Knowledge Base Links (Part 1 of 3)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
CPRI IP Core v12.0 Autorate Negotiation VHDL Testbench File Requires Modification	26-Jun-12	12.0		http://www.altera.com/support/kdb/solutions/fb52381.html
Rx MAP Buffer Might Overflow in 9.8304 Gbps CPRI IP Core Variations	26-Jun-12	12.0		http://www.altera.com/support/kdb/solutions/fb39649.html
CPRI IP Core Variations Configured with the All Mapping Mode Might Not Achieve Timing Closure	26-Jun-12	12.0		http://www.altera.com/support/kdb/solutions/fb47124.html
Some CPRI IP Core Variations Configured with the Advanced 1 Mapping Mode Might Not Achieve Timing Closure	26-Jun-12	12.0		http://www.altera.com/support/kdb/solutions/fb48244.html
Arria V GT CPRI IP Core Variations at 9.8304 Gbps Might Not Achieve timing Closure	26-Jun-12	12.0		http://www.altera.com/support/kdb/solutions/fb48244b.html
CPRI IP Core v11.1 SP2 Testbench .do Files for Arria V DUT Require Modification	27-Jun-12	11.1 SP2	12.0	http://www.altera.com/support/kdb/solutions/spr393860.html
Cannot Simulate Auto-Rate Negotiation in CPRI IP Core VHDL Models that Target Cyclone IV GX Devices	28-Jun-12	11.0	12.0	http://www.altera.com/support/kdb/solutions/spr372869.html
CPRI IP Cores That Target an Arria II GZ, Stratix IV, or Stratix V Device Fail Recovery Timing	9-Feb-12	11.1 SP1		http://www.altera.com/support/kdb/solutions/spr392393.html
CPRI MegaCore Function Ethernet Communication Fails with Mismatched cpri_clkout and cpu_clk Clocks	5-Dec-11	9.1 SP2	11.1 SP1	http://www.altera.com/support/kdb/solutions/spr391781.html
CPRI_ROUND_DELAY Register Value in CPRI IP Core is Wrong	17-Nov-11	11.0	11.1	http://www.altera.com/support/kdb/solutions/spr389637.html
CPRI MegaCore Function Fails Timing in Arria V GX Devices at Line Rates Above 3072 Mbps	11-Nov-11	9.1 SP2		http://www.altera.com/support/kdb/solutions/spr390671.html
CPRI MegaCore Function Variations That Target an Arria V or a Stratix V Device Require Additional Constraints	11-Nov-11	11.1		http://www.altera.com/support/kdb/solutions/spr391787.html
CPRI IP Core May Exhibit Hold Time Failures on Arria II GX Devices	16-Nov-11	11.0		http://www.altera.com/support/kdb/solutions/spr376356.html
Cannot Simulate Auto-Rate Negotiation for Some Line Rates in CPRI IP Core VHDL Models that Target Arria II GZ and Stratix IV GX Devices	9-Nov-11	11.0	11.1	http://www.altera.com/support/kdb/solutions/spr374182.html
CPRI_ROUND_DELAY Register Value in CPRI IP Core is Wrong by Eight Clock Cycles	9-Nov-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/spr372872.html

Table 8–2. CPRI MegaCore Function Errata Knowledge Base Links (Part 2 of 3)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
cpri_rx_cnt_sync port Description and Frame Synchronization FSM in CPRI MegaCore Function User Guide are Incorrect	9-Nov-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/spr360697.html
MII Interface Description in CPRI MegaCore Function v10.1 User Guide Contains Errors	9-Nov-11	10.1	11.0	http://www.altera.com/support/kdb/solutions/spr366538.html
CPRI MegaCore Function Protocol Version Default Value is Invalid	9-Nov-11	10.1	11.0	http://www.altera.com/support/kdb/solutions/spr365260.html
Erroneous File Names in CPRI 10.1 Testbench Description in CPRI MegaCore Function User Guide	9-Nov-11	10.1	11.0	http://www.altera.com/support/kdb/solutions/spr361738.html
Cannot Simulate CPRI MegaCore Function in Verilog HDL	9-Nov-11	10.1	11.0	http://www.altera.com/support/kdb/solutions/spr362394.html
CPU Interface Deadlocks After Attempt to Access Ethernet or HDLC Registers When CPRI MegaCore Function MII Interface Enabled	9-Nov-11	9.1 SP2	10.1 SP1	http://www.altera.com/support/kdb/solutions/spr361683.html
Errors in .mif File Names in CPRI IP Core Auto-Rate Negotiation Testbenches	9-Nov-11	10.1	10.1 SP1	http://www.altera.com/support/kdb/solutions/spr361398.html
CPRI MegaCore Function Testbench tb_altera_cpri.vhd Does Not Simulate	9-Nov-11	10.1	10.1 SP1	http://www.altera.com/support/kdb/solutions/spr361389.html
Cyclone IV GX CPRI IP Core REC Master Cannot Achieve Link Synchronization	9-Nov-11	10.1	10.1 SP1	http://www.altera.com/support/kdb/solutions/spr361235.html
Some CPRI MegaCore Function Variations Have Invalid cpri_clkout Frequency	9-Nov-11	10.1	10.1 SP1	http://www.altera.com/support/kdb/solutions/spr361057.html
Timing Violations in CPRI MegaCore Function for Some Device Families, Speed Grades, and Line Rates	8-Nov-11	9.1 SP2		http://www.altera.com/support/kdb/solutions/spr362221.html
CPRI MegaCore Function PRBS is Not Supported in Cyclone IV GX Devices	9-Nov-11	10.0	10.1	http://www.altera.com/support/kdb/solutions/spr348852.html
CPRI IP Core Auto-Rate Negotiation Does Not Support 614.4 Mbps Line Rate in Cyclone IV GX Devices	11-Nov-11	10.0	10.1	http://www.altera.com/support/kdb/solutions/spr392128.html
CPRI IP Core Simulation Testbench Does Not Support Cyclone IV GX Variations	9-Nov-11	10.0	10.1	http://www.altera.com/support/kdb/solutions/spr347421.html
Wrong Extended Rx Delay Measurement Clock Period in CPRI IP Core	9-Nov-11	10.0	10.1	http://www.altera.com/support/kdb/solutions/spr346619.html
Cannot Simulate CPRI IP Core Auto-Rate Negotiation in Verilog HDL With ModelSim 6.4b or Later	9-Nov-11	10.0	10.1	http://www.altera.com/support/kdb/solutions/spr346939.html

Table 8–2. CPRI MegaCore Function Errata Knowledge Base Links (Part 3 of 3)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
Warning Messages from Transceiver While Generating and Compiling CPRI MegaCore Function That Targets an Arria II GX, Arria II GZ, Cyclone IV GX, or Stratix IV GX Device	9-Nov-11	9.1 SP2		http://www.altera.com/support/kdb/solutions/spr346921.html
CPRI MegaCore Function v10.0 User Guide Does Not Contain Complete Instructions for Running the v10.0 Simulation Testbench	9-Nov-11	10.0	10.1	http://www.altera.com/support/kdb/solutions/spr347420.html
CPRI MegaCore Function CPU Interrupt Bit Always Set When Interrupts are Enabled	9-Nov-11	9.1 SP2	10.0	http://www.altera.com/support/kdb/solutions/spr344011.html
MII Interface Description in CPRI MegaCore Function v9.1SP1 User Guide Contains Errors	11-Nov-11	9.1 SP2	10.0	http://www.altera.com/support/kdb/solutions/spr392129.html
CPRI MegaCore Function User Guide Unavailable From MegaWizard Interface Info Link	9-Nov-11	9.1 SP2	10.0	http://www.altera.com/support/kdb/solutions/spr331125.html
MegaWizard Plug-In Manager Does Not Recognize Transceiver Instances Generated with CPRI Parameter Editor	9-Nov-11	9.1 SP2	10.0	http://www.altera.com/support/kdb/solutions/spr337350.html
CPRI Frame Synchronization Machine Unable to Return to XACQ1 from XSYNC1	9-Nov-11	9.1 SP2	10.0	http://www.altera.com/support/kdb/solutions/spr336136.html
Setup Time Violations Might Occur in 3072 Mbps CPRI IP Core Designs That Target an Arria II GX Device	11-Nov-11	9.1 SP2	10.0	http://www.altera.com/support/kdb/solutions/spr392126.html
CPRI MegaCore Function Does Not Support HardCopy IV GX Devices	11-Nov-11	9.1 SP2		http://www.altera.com/support/kdb/solutions/spr392127.html

9. CRC Compiler

Product Revision History

Table 9–1 shows the revision history for the CRC Compiler.

For more information about the new features, refer to the *CRC Compiler User Guide*.

Table 9–1. CRC Compiler Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	Maintenance release.
11.0	May 2011	Final support for Cyclone IV GX, Cyclone IV E, and Stratix IV devices.

Errata

For the most recent list of errata for the CRC Compiler, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

The following sections addresses known errata and documentation issues for the CRC Compiler. Errata are functional defects or errors, which may cause the CRC Compiler to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Not all issues affect all versions of the CRC Compiler.

Table 9–2 lists the errata for this IP core, the relevant versions, and links to the Knowledge Base.

Table 9–2. Errata Knowledge Base Links

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Testbench Directory Generated When You Create a Simulation Model	16-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr392321.html

10. Cyclone V Hard IP for PCI Express

Product Revision History

Table 10–1 shows the revision history for the Cyclone V Hard IP for PCI Express.

For more information about the new features, refer to the *Cyclone V Hard IP for PCI Express User Guide*.

Table 10–1. Stratix V Hard IP for PCI Express Revision History

Date	Version	Description
June 2012	12.0	■ Added ×1, ×4, and ×8 Gen1 support for Endpoints using the Avalon-MM interface ■ Added ×1 and ×4 Gen2 support for Endpoints using the Avalon-MM interface ■ Added support for dynamic reconfiguration of transceiver settings ■ Added support for VHDL simulation
February 2012	11.1 SP2	Verified with the Quartus II software v11.1 SP2.
December 2011	11.1 SP1	Verified with the Quartus II software v11.1 SP1.
November	11.1	First release.

Errata

For a recent list of errata and affected versions of the Cyclone V Hard IP for PCI Express IP core, refer to the Altera Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the Cyclone V Hard IP for PCI Express.

Table 10–2 lists the errata for the Hard IP for PCI Express, the relevant software releases, and links to the Knowledge Base.

Table 10–2. Hard IP for PCI Express Errata Knowledge Base Links (Part 1 of 2)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
PCI Express VHDL Example Design Simulation Fails	8-Feb-12	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr393995.html
Reconfiguration Ports Not Available for Arria V and Cyclone V Hard IP for PCI Express IP Cores	23-Jan-12	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/fb34064.html

Table 10–2. Hard IP for PCI Express Errata Knowledge Base Links (Part 2 of 2)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
The User Guides for PCI Express Do Not Document How a Variant Handles the Address Translation and Reserved Bits of a TLP Header	17-Nov-11	Version 11.0	Version 12.0	http://www.altera.com/support/kdb/solutions/spr385731.html
Hard IP for PCI Express User Guides Shows Incorrect Value for Receiver Detect Capacitor	03-July-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb61601.html
Arria V and Cyclone V Hard IP for PCI Express IP Cores Do Not Downtrain to x1	13-June-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb57305.html
Multi-Function Parameter Is Incorrectly Set in Arria V and Cyclone V Hard IP for PCI Express IP Cores	08-June-12	Version 11.1		thttp://www.altera.com/support/kdb/solutions/fb54277.html
VHDL Compilation Fails for Arria V and Cyclone V Hard IP for PCI Express	8-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr390424.html
Advanced Error Reporting (AER) and ECRC Not Available for Arria V and Cyclone V Hard IP for PCI Express	9-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr392030.html

11. DDR and DDR2 SDRAM Controller Compiler

Product Revision History

Table 11–1 shows the revision history for the DDR and DDR2 SDRAM Controller Compiler.

For more information about the new features, refer to the *DDR and DDR2 SDRAM Controller Compiler User Guide*.

Table 11–1. DDR and DDR2 SDRAM Controller Compiler Revision History

Version	Date	Description
11.0	May 2011	Maintenance release.
10.1	December 2010	Maintenance release.
10.0	July 2010	Maintenance release.

Errata

For the most recent list of errata for the DDR and DDR2 SDRAM Controller Compiler, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

12. DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP

Product Revision History

Table 12–1 shows the revision history for the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP MegaCore function.

For more information about the new features, refer to the *External Memory Interface Handbook*.

Table 12–1. DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP MegaCore Function Revision History

Version	Date	Description
12.0	June 2012	Verified with the Quartus II software v12.0
11.1 SP2	February 2012	Verified with the Quartus II software v11.1 SP2
11.1	November 2011	Verified with the Quartus II software v11.1
11.0 SP1	July 2011	Verified with the Quartus II software v11.0 SP1
11.0	May 2011	Added new controller features, including data-reordering capability

Errata

For the most recent list of errata for the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP MegaCore function, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

The following sections addresses known errata and documentation issues for the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP MegaCore function. Errata are functional defects or errors, which may cause the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Not all issues affect all versions of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP MegaCore function.

Table 12–2 lists the errata for this IP core, the relevant versions, and a link to the Knowledge Base.

Table 12–2. Errata Knowledge Base Links (Part 1 of 3)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset	14-Feb-12	Version 10.0	Version 10.0	http://www.altera.com/support/kdb/solutions/spr390362.html
Gate Level Simulation Fails	14-Feb-12	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390366.html
Generate Simulation Model Option Gets Disabled	15-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390097.html
Need to Manually Connect Memory Model	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr375501.html
Reduced Clock Rate Specification for Column and Row I/Os	14-Sep-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr352005.html
ECC Interrupt Function Not On by Default	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr379914.html
VHDL Example Driver Fails in Simulation	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr372157.html
Half Rate Bridge Not Supported in Simulation	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr374150.html
Memory Controller Returns Wrong Data	14-Sep-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr354765.html
pin_assignments.tcl Contains Incorrect Pin Names in Qsys Systems	14-Sep-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr359436.html
SOPC Builder and Qsys Do Not Support Full-Rate DDR with HPC I in Simulation	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr375503.html
Error Related to Incorrect Syntax of Type Conversion	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr375513.html
System Timestamp Mismatch Warning Message	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr373045.html
VCS Simulation Fails and Reports that Module was Previously Declared	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr374162.html
Warning Messages Reporting Ignored SDC Constraints	12-Sep-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr359216.html
ECC Registers Not Accessible from Controller Register Map	12-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr379092.html
SOPC Builder Not Supported for DDR SDRAM Controller with ALTMEMPHY	12-Sep-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr343582.html
RTL Simulation May Fail When Dedicated Memory Clock Outputs Are Selected	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390365.html

Table 12–2. Errata Knowledge Base Links (Part 2 of 3)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Cyclone III Speed Grade Support for Full-Rate DDR2 SDRAM Memory Specification	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390125.html
Simulating with the VCS Simulator	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390371.html
Half-Rate Clock Not Connected When Clock Sharing is Enabled	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390356.html
Memory Presets Contain Some Incorrect Memory Timing Parameters	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390368.html
Wrong Default Value	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390357.html
DQS and DQSn Signals Generate Extra Pulse	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390357.html
Using Merging Feature	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390121.html
Simulating with the NCSim Software	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390370.html
Designs with Eight Chip Selects Fail Compilation	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390361.html
Refresh to Precharge Command Timing Violation	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390122.html
Postamble Calibration Scheme in Sequencer Violates Timing	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390354.html
Failure to Regenerate 9.0 Designs in Silent Mode	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390124.html
Power-Down Entry Command Timing Violation	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390123.html
Error in Board Settings GUI	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390120.html
VHDL Simulation Fails When DDR CAS Latency 2.0 or 2.5 Is Selected	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390367.html
Generate Simulation Model Option Gets Disabled	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390359.html
CSR Address 0×005 and 0×006 Contents Cannot be Accessed	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390355.html
SOPC Builder Does Not Recognize Decimal Points	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390363.html
DDR Controller Designs in AFI Mode with Memory Burst Length of 2 Fail in Simulation	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390360.html

Table 12–2. Errata Knowledge Base Links (Part 3 of 3)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Timing Violation In Half-Rate Bridge Enabled Designs	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390358.html
Mimic Path Incorrectly Placed	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr243889.html

13. DDR3 SDRAM Controller with ALTMEMPHY IP

Product Revision History

Table 13–1 shows the revision history for the DDR3 SDRAM Controller with ALTMEMPHY IP MegaCore function.

For more information about the new features, refer to the *External Memory Interface Handbook*.

Table 13–1. DDR3 SDRAM Controller with ALTMEMPHY IP MegaCore Function Revision History

Version	Date	Description
12.0	June 2012	Verified with the Quartus II software v12.0
11.1 SP2	February 2012	Verified with the Quartus II software v11.1 SP2
11.1	November 2011	Verified with the Quartus II software v11.1
11.0 SP1	July 2011	Verified with the Quartus II software v11.0 SP1
11.0	May 2011	Added new controller features, including data-reordering capability

Errata

For the most recent list of errata for the DDR3 SDRAM Controller with ALTMEMPHY IP MegaCore function, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

The following sections addresses known errata and documentation issues for the DDR3 SDRAM Controller with ALTMEMPHY IP MegaCore function. Errata are functional defects or errors, which may cause the DDR3 SDRAM Controller with ALTMEMPHY IP MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Not all issues affect all versions of the DDR3 SDRAM Controller with ALTMEMPHY IP MegaCore function.

Table 13–2 lists the errata for this IP core, the relevant versions, and a link to the Knowledge Base.

Table 13–2. New Table, w/entries from ddr/2+alt chapter

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset	14-Feb-12	Version 10.0	Version 10.0	http://www.altera.com/support/kdb/solutions/spr390362.html
For DDR3 SDRAM Controller with UniPHY and DDR3 SDRAM Controller with ALTMEMPHY IP, Devices Faster than 533MHz Require Manual Derating	24-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr360438.html
DDR3 ODT Fails in Simulation with Denali for DDR2 and DDR3 SDRAM Controller with UniPHY and DDR3 SDRAM Controller with ALTMEMPHY IP	24-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr371466.html
Generate Simulation Model Option Gets Disabled	15-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390097.html
Memory Timing Violation During Activate Read Auto-Precharge to Refresh/Activate	15-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390095.html
Address Mirroring Not Supported by Memory Simulation Model	15-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390107.html
Generate Simulation Model Option Gets Disabled	15-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390097.html
Memory Preset Parameters Do Not get Updated	15-Nov-11	Version 9.0		http://www.altera.com/support/kdb/solutions/spr390108.html
Unexpected Timing Results in Design With Both ALTMEMPHY and UniPHY	15-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr390608.html
ECC Interrupt Function Not On by Default	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr379914.html
VHDL Example Driver Fails in Simulation	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr372157.html
Half Rate Bridge Not Supported in Simulation	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr374150.html
Memory Controller Returns Wrong Data	14-Sep-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr354765.html
pin_assignments.tcl Contains Incorrect Pin Names in Qsys Systems	14-Sep-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr359436.html
Error Related to Incorrect Syntax of Type Conversion	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr375513.html
System Timestamp Mismatch Warning Message	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr373045.html

Table 13–2. New Table, w/entries from ddr/2+alt chapter

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
VCS Simulation Fails and Reports that Module was Previously Declared	14-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr374162.html
Warning Messages Reporting Ignored SDC Constraints	12-Sep-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr359216.html
ECC Registers Not Accessible from Controller Register Map	12-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr379092.html
Generate Simulation Model Option Gets Disabled	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390359.html
Half-Rate Clock Not Connected When Clock Sharing is Enabled	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390356.html
Using Merging Feature	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390121.html
Designs with Eight Chip Selects Fail Compilation	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390361.html
Refresh to Precharge Command Timing Violation	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390122.html
Failure to Regenerate 9.0 Designs in Silent Mode	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390124.html
Power-Down Entry Command Timing Violation	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390123.html
Error in Board Settings GUI	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390120.html
CSR Address 0×005 and 0×006 Contents Cannot be Accessed	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr390355.html

14. DDR2, DDR3, and LPDDR2 SDRAM Controller with UniPHY

Product Revision History

Table 14–1 shows the revision history for the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

For more information about the new features, refer to the *External Memory Interface Handbook*.

Table 14–1. DDR2 and DDR3 SDRAM Controller with UniPHY Revision History

Version	Date	Description
12.0	June 2012	■ Added LPDDR2 support ■ Added shadow register support ■ Added new EMIF Toolkit ■ Added compilation support for Arria V soft interfaces ■ Added compilation support for Cyclone V soft and hard interfaces
11.1 SP2	February 2012	■ Added POF support for Stratix V 800MHz DDR3 ■ Added EMIF Toolkit support for Stratix V ■ Added automatic dynamic tracking for frequencies above 533MHz ■ Added compilation support for Cyclone V hard memory interface
11.1	November 2011	■ Added support for Arria V devices ■ Added support for Cyclone V devices ■ Added quarter-rate support for Stratix V devices
11.0 SP1	July 2011	Added quarter-rate support and 800MHz support for DDR3
11.0	May 2011	■ Added new controller features, including data-reordering capability ■ Added support for DDR3L on Stratix V devices—the same specification as DDR3, but a low-power version using 1.35 V I/Os ■ Added support for optional new efficiency monitor and protocol checker in UniPHY EMIF toolkit

Errata

For the most recent list of errata for the DDR2, DDR3, and LPDDR2 SDRAM Controller with UniPHY IP core, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

The following sections addresses known errata and documentation issues for the DDR2, DDR3, and LPDDR2 SDRAM Controller with UniPHY IP core. Errata are functional defects or errors, which may cause the IP cores to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Not all issues affect all versions of the DDR2, DDR3, and LPDDR2 SDRAM Controller with UniPHY IP core.

Table 14–2 lists the errata for this IP core, the relevant versions, and a link to the Knowledge Base.

Table 14–2. Errata Knowledge base Links (Part 1 of 9)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Compilation Fails When Bonding Feature is Enabled	14-Feb-12	Version 11.1 SP2	Version 12.0	http://www.altera.com/support/kdb/solutions/spr393625.html
Designs Targeting Stratix V ES Devices May Fail Timing in TimeQuest	14-Feb-12	Version 11.1 SP2	Version 12.0	http://www.altera.com/support/kdb/solutions/spr394081.html
Calibration May Fail Without Issuing CAL_FAIL Signal	14-Feb-12	Version 11.1 SP2	Version 12.0	http://www.altera.com/support/kdb/solutions/spr394052.html
DDR3L Designs on Stratix V ES Devices May Fail in Assembler	14-Feb-12	Version 11.1 SP2	Version 12.0	http://www.altera.com/support/kdb/solutions/spr394029.html
Example Design for Arria V with Hard Memory Interface Uses Wrong Clock	14-Feb-12	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/fb31983.html
Error Migrating Design from 11.0 to 11.0 SP1 for DDR2 and DDR3 SDRAM Controller with UniPHY	24-Nov-11	Version 11.0 SP1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr379159.html
ECC and CSR Designs Fail Timing	24-Nov-11	Version 11.0	Version 12.0	http://www.altera.com/support/kdb/solutions/spr379191.html
Non-leveled DDR2 Topology Fails Timing with Stratix V Devices for DDR2 and DDR3 SDRAM Controller with UniPHY	24-Nov-11	Version 11.0 SP1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr378814.html
NativeLink Simulation in UniPHY External Memory Interfaces fail for VHDL Output	18-Nov-11	Version 10.0	Version 12.0	http://www.altera.com/support/kdb/solutions/spr362558.html
Cannot Share One PLL/DLL/OCT Master with Multiple Slaves in Qsys for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 12.0	http://www.altera.com/support/kdb/solutions/spr372587.html
NativeLink Simulation for UniPHY External Memory Interfaces fails for VHDL Output	18-Nov-11	Version 10.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr362559.html
Simulation with NC Sim or Riviera-PRO Fails with an Elaboration Error for UniPHY External Memory Interfaces	18-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr377595.html

Table 14–2. Errata Knowledge base Links (Part 2 of 9)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
VHDL-Generated Fileset Can Encounter Synthesis Problems for UniPHY External Memory Interfaces	18-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr377804.html
Error Message for Auto Power Down Cycles Does Not Indicate Valid Range	15-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr392213.html
Compilation Failure with UniPHY Cores Targeting Arria V and Cyclone V	15-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr392124.html
Controller Bonding is Not Available in the Hard Memory Interface	15-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr391384.html
Some DQ Group Locations Are Not Usable in Cyclone V	15-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr388622.html
Warning Messages About afi_rdata_valid, afi_rdata_en, afi_rdata_en_full	15-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr388691.html
SOPC Builder Issues Erroneous Error Message	15-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr387451.html
UniPHY EMIF Toolkit Reports Narrow Data Valid Window	15-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr387075.html
For DDR2 and DDR3 SDRAM Controller with UniPHY, EMIF Toolkit Reports Incorrect CAS Latency for 10.1 IP Opened in 11.0	24-Nov-11	Version 11.0	Version 12.0	http://www.altera.com/support/kdb/solutions/spr371361.html
For V-series Families, VHDL is Not Supported When Read DQS Tracking is Enabled	14-Feb-12	Version 11.1 SP1	Version 11.1 SP2	http://www.altera.com/support/kdb/solutions/spr392499.html
Fitter Error Occurs When Read DQS Tracking is Enabled	14-Feb-12	Version 11.1 SP1	Version 11.1 SP2	http://www.altera.com/support/kdb/solutions/spr392718.html
Cyclone V Hard Memory Interface Does Not provide Fitter Support	15-Nov-11	Version 11.1	Version 11.1 SP2	http://www.altera.com/support/kdb/solutions/spr387776.html
Invalid Maximum Avalon-MM burst length Value Causes Simulation Failure	15-Nov-11	Version 11.1	Version 11.1 SP2	http://www.altera.com/support/kdb/solutions/spr392105.html
Incorrect Multiple Port Address Width	15-Nov-11	Version 11.1	Version 11.1 SP2	http://www.altera.com/support/kdb/solutions/spr391989.html
No Error Message is Displayed for Invalid Configuration	15-Nov-11	Version 11.1	Version 11.1 SP1	http://www.altera.com/support/kdb/solutions/spr391719.html
Self-refresh Not Working Properly for Single-rank DDR3 DIMMs	15-Nov-11	Version 11.1	Version 11.1 SP1	http://www.altera.com/support/kdb/solutions/spr390482.html

Table 14–2. Errata Knowledge base Links (Part 3 of 9)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
In DDR2 and DDR3 SDRAM Controller with UniPHY, Example Designs Without DM Pins Enabled Will Fail	24-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr370303.html
DDR2 and DDR3 SDRAM Controller with UniPHY User Guide Contains Imprecise Clock Information	24-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr377292.html
DDR2 and DDR3 SDRAM Controller with UniPHY User Guide Contains Incorrect Clock Information	24-Nov-11	Version 10.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr350117.html
Efficiency Monitor Latency Values Are Incorrect for DDR2 and DDR3 SDRAM Controller with UniPHY and RLDRAM II Controller with UniPHY	23-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr376056.html
Must Enable Support for Nios II ModelSim Flow in GUI for DDR2 and DDR3 SDRAM Controller with UniPHY and RLDRAM II Controller with UniPHY	23-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr371218.html
Example Design Simulation for UniPHY External Memory Interfaces May Fail in NC Sim	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr371331.html
Simulation Fails for UniPHY External Memory Interfaces when Generating VHDL for Designs Using Nios II-based Sequencer	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr373105.html
PLL Master Required for Simulation of PLL Slave for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr374852.html
Conduit Error Messages Displayed in Qsys for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr372446.html
Simulation Fails for UniPHY External Memory Interfaces with “Undefined System Task Call” Error	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr373731.html
Simulation of Example Designs Can Fail or Produce Warnings for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr368146.html

Table 14–2. Errata Knowledge base Links (Part 4 of 9)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
DDR3 ODT Fails in Simulation with Denali for DDR2 and DDR3 SDRAM Controller with UniPHY and DDR3 SDRAM Controller with ALTMEMPHY IP	24-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr371466.html
Simulation Fails When Enable Auto Error Correction Option Enabled	24-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr375505.html
ECC and CSR Designs May Fail in Simulation or Hardware	24-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr375499.html
Multi-cast Write Control Not Supported	24-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr375506.html
UniPHY CSR Ports Not Functioning Correctly for External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr377353.html
Example Project Fails to Simulate When HardCopy Compatibility is Enabled for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr375477.html
ModelSim Waveform Viewer for UniPHY External Memory Interfaces Shows Only clk and reset Signals	18-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr375193.html
Minimum Pulse Width Timing Failures for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr374717.html
For DDR3 SDRAM Controller with UniPHY and DDR3 SDRAM Controller with ALTMEMPHY IP, Devices Faster than 533MHz Require Manual Derating	24-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr360438.html
For DDR2 and DDR3 SDRAM Controller with UniPHY, SOPC Builder Designs Suffer Low Efficiency	24-Nov-11	Version 10.0	Version 11.0	http://www.altera.com/support/kdb/solutions/spr347821.html
Incorrect Clock Uncertainty in UniPHY External Memory Interfaces	18-Nov-11	Version 10.0	Version 11.0	http://www.altera.com/support/kdb/solutions/spr344172.html
Example Designs for UniPHY External Memory Interfaces May Not Compile for IP Cores from Earlier Versions	18-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr357422.html

Table 14–2. Errata Knowledge base Links (Part 5 of 9)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
SOPC Builder-generated Systems Cannot Serve as Top-Level Design for UniPHY External Memory Interfaces	18-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr356433.html
Compilation Fails for UniPHY External Memory Interfaces if Synthesis Fileset is Mixed with Example Project Files	18-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr359597.html
Warning Messages Displayed for UniPHY External Memory Interfaces When Compiling for Stratix V Devices	18-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr358219.html
Error in Graphical Display of DQ Calibration Margin in EMIF Toolkit for DDR2 and DDR3 SDRAM Controller with UniPHY	24-Nov-11	Version 10.1	Version 10.1 SP1	http://www.altera.com/support/kdb/solutions/spr363427.html
DDR2 and DDR3 SDRAM Controller with UniPHY Example Design Fails as a Slave	24-Nov-11	Version 10.0	Version 10.1	http://www.altera.com/support/kdb/solutions/spr346620.html
For DDR2 and DDR3 SDRAM Controller with UniPHY, Designs Without Leveling Fail in Stratix V Devices	24-Nov-11	Version 10.0	Version 10.1	http://www.altera.com/support/kdb/solutions/spr345561.html
In DDR2 and DDR3 SDRAM Controller with UniPHY, Selecting VHDL Gives a Verilog HDL IP Core	24-Nov-11	Version 10.0	Version 10.1	http://www.altera.com/support/kdb/solutions/spr345460.html
BSF File Not Generated for UniPHY External Memory Interfaces	23-Nov-11	Version 10.0	Version 10.1	http://www.altera.com/support/kdb/solutions/spr346650.html
DDR3 Quarter-Rate Is Not Supported for Cyclone V Devices	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb62265.html
Possible Calibration Error for DDR2 and DDR3 Interfaces on Arria V, Cyclone V, and Stratix V Devices	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb61220.html
Center PLL in Arria V Cannot Drive Two Independent PHY Clock Networks	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb60761.html
Memory Controller May Become Unresponsive for LPDDR2 Interfaces Using Deep Power-Down Mode on Arria V or Cyclone V Devices	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb60760.html

Table 14–2. Errata Knowledge base Links (Part 6 of 9)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Cannot Generate DDR3 RDIMM IP for Stratix IV or Stratix V with RC8–RC15 Set to Non-Zero Values	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb60564.html
Low Frequency Limit of 167 MHz for DDR2 and LPDDR2 on Arria V and Cyclone V Devices	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb60664.html
Deep Power Down Issue With LPDDR2 Interfaces on Cyclone V Devices	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb58590.html
Board Skew Analysis Is Incorrect for Arria V and Cyclone V Devices	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb56762.html
Arria V Soft DDR2 Interfaces Support Simulation and Compilation Only	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb56511.html
DQS# Enable Option Must be Enabled for LPDDR2 Interfaces	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb56447.html
VHDL Post-Fit Simulation Failure on Stratix V Devices	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb56374.html
Warning Message Displayed When Driving User Logic with Custom PLL in Hard Memory Interface	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb56283.html
Arria V Soft Controller May Not Meet Frequency Targets if CSR or ECC Enabled	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb56198.html
EMIF Toolkit Will Not Link to Designs Created in Qsys	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb55124.html
PHY Clock Tree Not Driven by Optimal PLL Output Counters	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb55089.html
LPDDR2 Timing Closure Problem with Arria V Devices	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb54932.html
No-Fit in DDR3 Interfaces Due to mem_ck Assignments	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb54468.html
ECC Logic Always Enabled in Controller when CSR is Enabled	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb53788.html
Arria V and Cyclone V Hard Memory Controller Options May Not Function Correctly for Interfaces with 2 Chip Selects	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb53386.html
Soft Controller May Not Meet Timing When Data Reordering is Enabled	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb52805.html

Table 14–2. Errata Knowledge base Links (Part 7 of 9)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
tCCD=1 for LPDDR2-S4 Devices Does Not Meet Minimum tCCD of 2 Cycles	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb51930.html
DDR3 Interfaces with Multiple mem_ck signals May Produce No-Fit Errors	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb51548.html
Warning Messages Displayed in TimeQuest	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb51089.html
Possible to Select Unsupported Device Family for LPDDR2 Interface	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb50948.html
Generation Error or VHDL Simulation Failure for LPDDR2 Interface	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb50042.html
Possible Internal Error with Arria V or Cyclone V Designs Using Hard Memory Controller	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb49167.html
RTL Modification Required for Top/Bottom Bonding on Arria V and Cyclone V Devices	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb48965.html
EMIF Toolkit Will Not Link to Projects Containing In-System Memory Editor	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb48648.html
Illegal Speed Grade Error with Arria V and Cyclone V Devices	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb48632.html
Postfit Simulation of UniPHY Hard Memory Interfaces is Not Supported for Arria V Devices	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb46876.html
Simulation Example Design Fails and Produces Warnings	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb44572.html
Calibration Failure Occurs when RELEASE_CLEARS_BEFORE_TRI_STATES is On	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb40520.html
User Refresh Limitation in Arria V and Cyclone V Hard Memory Interface	14-Feb-12	Version 11.1		http://www.altera.com/support/kdb/solutions/fb31428.html
Using Burst Merging Feature for DDR2 and DDR3 SDRAM Controller with UniPHY	24-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr348355.html
Fitter Error When Compiling DDR2 Designs Below 240MHz in DDR2 and DDR3 SDRAM Controller with UniPHY	24-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr373172.html
Memory Controller Uses 1T Memory Timing	24-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr376041.html

Table 14–2. Errata Knowledge base Links (Part 8 of 9)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Simulation Fails for Memory Additive CAS Latency Settings > 0	24-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr375274.html
For DDR2 and DDR3 SDRAM Controller with UniPHY, Quartus II Software Cannot Read .mif File for PLL	24-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr346588.html
Error Occurs When Running Simulation Example Design in ModelSim	15-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr387730.html
DDR2 and DDR3 SDRAM Controller with UniPHY Simulation Fails in Riviera	24-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr346655.html
Efficiency Monitor Statistics Incorrect for Initial Sample in DDR2 and DDR3 SDRAM Controller with UniPHY and RLDRAM II Controller with UniPHY	23-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr374202.html
Global Signal Assignments for UniPHY External Memory Interfaces Not Applied	23-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr345461.html
Simulation Fails with PLL Clocks Out of Synchronization for UniPHY External Memory Interfaces	23-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr352405.html
Example Design Can Fail For Certain Parameterizations of QDR II and QDR II+ SRAM Controller with UniPHY and DDR2 and DDR3 SDRAM Controller with UniPHY	23-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr371214.html
Error Messages for UniPHY External Memory Interfaces in ModelSim Flow for Eclipse	18-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr375252.html
Cannot Launch MegaWizard Plug-In Manager by Opening Example Design for UniPHY External Memory Interfaces	18-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr357643.html
Higher Delays and Skews Expected for UniPHY External Memory Interfaces Corner I/Os in Stratix V Devices	18-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr351007.html
UniPHY IP Generation for External Memory Interfaces Fails if the Quartus II Installation Path Contains a Space	18-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr376172.html

Table 14–2. Errata Knowledge base Links (Part 9 of 9)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Unable to Directly Recompile Quartus II version 10.1 Design for UniPHY External Memory Interfaces in Quartus II version 11.0	18-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr373335.html
Compilation of a UniPHY Example Design Can Produce Warnings for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr367353.html
How to Use UniPHY-based Memory IP with SOPC Builder	18-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr373304.html
Reset Synchronizer for UniPHY External Memory Interfaces May Cause Design to Fail Timing when generated in SOPC Builder or Qsys	18-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr360104.html
Erroneous Timing Failures in Designs Containing Both UniPHY and ALTMEMPHY Instantiations for External Memory Interfaces	18-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr377893.html
Segmentation Fault During Elaboration with ModelSim SE	15-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr392043.html
VCS-MX Simulation with Simulation Script vcsmx_setup.sh Fails at 0ns	15-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr388472.html

15. FFT

Product Revision History

Table 15–1 shows the revision history for the FFT MegaCore function.

For more information about the new features, refer to the *FFT MegaCore Function User Guide*.

Table 15–1. FFT MegaCore Function Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	■ Preliminary suport for Arria V and Cyclone V devices.
11.0	May 2011	■ Final support for Arria II GX, Arria II GZ, Cyclone III LS, and Cyclone IV GX devices. ■ HardCopy Compilation support for HardCopy III, HardCopy IV E, and HardCopy IV GX devices.

Errata

For the most recent list of errata for the FFT MegaCore function, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the FFT MegaCore function.

16. FIR Compiler

Revision History

Table 16–1 shows the revision history for the FIR Compiler.

For information about the new features, refer to the *FIR Compiler User Guide*.

Table 16–1. FIR Compiler Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	Maintenance release.
11.0	May 2011	■ Final support for Arria II GX, Arria II GZ, Cyclone III LS, and Cyclone IV GX devices. ■ HardCopy Compilation support for HardCopy III, HardCopy IV E, and HardCopy IV GX devices. ■ Updated HardCopy initialization information in Appendix A, FIR Compiler Supported Device Structures.

Errata

For the most recent list of errata for the FIR Compiler, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the FIR Compiler.

17. FIR Compiler II

Product Revision History

Table 17–1 shows the revision history for the FIR Compiler II.

For information about the new features, refer to the *FIR Compiler II User Guide*.

Table 17–1. FIR Compiler II Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	Updated resource utilization and performance information for Stratix V devices.
11.0	May 2011	Added resource utilization and performance information for Stratix V devices.

Errata

For the most recent list of errata for the FIR Compiler II, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the FIR Compiler II.

18. Interlaken

Product Revision History

Table 18–1 shows the revision history for the Interlaken MegaCore function.

For information about the new features, refer to the *Interlaken MegaCore Function User Guide*.

Table 18–1. Interlaken MegaCore Function Revision History

Version	Date	Description
12.0	June 2012	Maintenance release.
11.1	November 2011	■ Added parameterizable or dynamically configurable BurstMax and BurstShort. ■ Added parameterizable exposed calendar pages and number of pages. ■ Added global reset signal.
11.0	May 2011	Maintenance release.

Errata

For a current list of errata that affect the Interlaken MegaCore function, refer to the Knowledge Base web page.

Not all issues affect all versions of the Interlaken MegaCore function.

For Qsys errata, which might affect the Interlaken MegaCore function and other IP cores, refer to the *Quartus II Software Release Notes*.

Table 18–2 lists the errata for the Interlaken MegaCore function, the relevant software releases, and links to the Knowledge Base.

Table 18–2. Interlaken MegaCore Function Errata Knowledge Base Links (Part 1 of 2)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
SDC File Provided With Interlaken MegaCore Function Includes Overly Agressive Timing Path Cuts	11-Nov-11	10.1	11.0	http://www.altera.com/support/kdb/solutions/spr371802.html
Interlaken MegaCore Function 10.3125-Gbps Variation With Transceivers Runs at Incorrect Lane Rate	11-Nov-11	10.1	11.0	http://www.altera.com/support/kdb/solutions/spr360777.html
Critical Warnings for Interlaken MegaCore Function 12- and 20-Lane Variations Without Transceivers	11-Nov-11	10.1		http://www.altera.com/support/kdb/solutions/spr357506.html

Table 18–2. Interlaken MegaCore Function Errata Knowledge Base Links (Part 2 of 2)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
rst_rxd Warning for Interlaken MegaCore Function 10- and 20-Lane Variations With Transceivers	11-Nov-11	10.1	11.1	http://www.altera.com/support/kdb/solutions/spr357361.html
Compiler Warnings When Transceivers are Excluded From Interlaken MegaCore Function	11-Nov-11	10.1		http://www.altera.com/support/kdb/solutions/spr356574.html
Aldec Riviera-PRO Simulator Cannot Simulate Interlaken 8-Lane Variation	11-Nov-11	10.1		http://www.altera.com/support/kdb/solutions/spr359115.html
C106 Warnings for Interlaken MegaCore Function 10- and 20-Lane Variations With Transceivers	11-Nov-11	10.1		http://www.altera.com/support/kdb/solutions/spr358593.html

19. Interlaken PHY

Revision History

Table 19–1 shows the revision history for the Interlaken PHY IP core.

For more information about the new features, refer to the "*Interlaken PHY IP Core*" chapter in the *Altera Transceiver PHY IP Core User Guide*.

Table 19–1. Interlaken PHY Revision History

Version	Date	Description
12.0	June 2012	■ Added support for custom, user-defined, data rates. ■ Added the following QSF settings for all transceivers: ■ XCVR_TX_PRE_EMP_2ND_POST_TAP_USER ■ XCVR_TX_PRE_EMP_PRE_TAP_USER ■ Added 11 new settings for GT transceivers.
11.0	May 2011	Verified with the Quartus II software v11.0.

Errata

For the most recent list of errata for the Interlaken PHY IP core, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Table 19–2 lists the errata for the Interlaken PHY IP Core, the relevant software releases, and links to the Knowledge Base.

Table 19–2. Interlaken PHY IP Core Errata Knowledge Base Links

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Simulation of 10GBASE-R, Custom, Interlaken, Low Latency, PCI Express PIPE, and XAUI Transceiver PHY IP Cores Fails for Stratix V if You Use ModelSim With Mixed Languages	11-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr36210.html

20. IP Compiler for PCI Express

Product Revision History

Table 20–1 shows the revision history for the IP Compiler for PCI Express.

For complete information about the new features, refer to the IP Compiler for PCI Express User Guide.

Table 20–1. IP Compiler for PCI Express Revision History

Version	Date	Description
12.0	June 2012	Maintenance release.
11.1 SP2	February 2012	Maintenance release.
11.1 SP1	December 2011	Maintenance release.
11.1	November 2011	Maintenance release.
11.0 SP1	July 2011	Maintenance release.
11.0	May 2011	■ Name change to *IP Compiler for PCI Express*. ■ Removed support for Stratix V devices. Stratix V device support is provided by the *Stratix V Hard IP for PCI Express*, and not by the *IP Compiler for PCI Express*. ■ Added Qsys support.

Errata

For the most recent list of errata for the IP Compiler for PCI Express, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the IP Compiler for PCI Express.

Table 20–2 lists the errata for the IP Compiler for PCI Express, the relevant software versions, and links to the Knowledge Base.

Table 20–2. IP Compiler for PCI Express Errata Knowledge Base Links (Part 1 of 5)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
Migrating to a New Version of the IP Compiler for PCI Express Requires Removal of _serdes.v or _serdes.vhd File	27-Jun-12	11.0		http://www.altera.com/support/kdb/solutions/fb43382.html
IP Compiler for PCI Express User Guide Does Not Accurately Describe Non-Posted tx_cred Offset	27-Jun-12	11.0		http://www.altera.com/support/kdb/solutions/fb39781.html

Table 20–2. IP Compiler for PCI Express Errata Knowledge Base Links (Part 2 of 5)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
IP Compiler for PCI Express Responds to User Write Request to Upper Dword With Incorrect Byte Enable	27-Jun-12	11.1	12.0	http://www.altera.com/support/kdb/solutions/fb34024.html
IP Compiler for PCI Express User Guide Erroneous Description of Flow Control Protocol Error	24-Jan-12	11.0		http://www.altera.com/support/kdb/solutions/fb33499.html
Errors in Figures B-8 and B-9 in IP Compiler for PCI Express v11.0 User Guide	17-Nov-11	11.0		http://www.altera.com/support/kdb/solutions/spr392519.html
IP Compiler for PCI Express User Guide Table 1-9 Erroneously Indicates ECC Support is Available in Variations That Target an Arria II GX Device	17-Nov-11	9.1 SP2		http://www.altera.com/support/kdb/solutions/spr391840.html
The Hard IP Implementation of the PCI Express Compiler May Be Unable to Exit the Disable State at the Gen2 Rate	17-Nov-11	9.0		http://www.altera.com/support/kdb/solutions/spr391690.html
Cannot Modify Maximum Payload Size in IP Compiler for PCI Express Parameter Editor	5-Dec-11	9.1	11.1 SP1	http://www.altera.com/support/kdb/solutions/spr391678.html
Cannot Modify RX Buffer Settings in IP Compiler for PCI Express Parameter Editor	5-Dec-11	9.1	11.1 SP1	http://www.altera.com/support/kdb/solutions/spr391677.html
Missing gxb_powerdown and pll_powerdown Input Signals in Qsys-Generated IP Compiler for PCI Express Variations	17-Nov-11	11.0		http://www.altera.com/support/kdb/solutions/spr391608.html
Some IP Compiler for PCI Express Variations That Target a HardCopy IV GX Device Cannot Close Timing	5-Dec-11	11.1	11.1 SP1	http://www.altera.com/support/kdb/solutions/spr391398.html
Qsys-Generated IP Compiler for PCI Express May Send Deassert_INTA Message While Interrupt is Still Asserted	17-Nov-11	11.0	11.1	http://www.altera.com/support/kdb/solutions/spr389991.html
The User Guides for PCI Express Do Not Document How a Variant Handles the Address Translation and Reserved Bits of a TLP Header	17-Nov-11	11.0		http://www.altera.com/support/kdb/solutions/spr385731.html
SOPC Builder Generated IP Compiler for PCI Express Variations Have Wrong Default Value for test_in[5]	17-Nov-11	11.0		http://www.altera.com/support/kdb/solutions/spr385496.html

Table 20–2. IP Compiler for PCI Express Errata Knowledge Base Links (Part 3 of 5)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
IP Compiler for PCI Express Endpoint in Disable State Does Not Complete Sending Final TS1 Before Transmitting Electrical Idle	17-Nov-11	11.0		http://www.altera.com/support/kdb/solutions/spr383193.html
Streaming an MSI Request to the IP Compiler for PCI Express Design Example ICM Module While Streaming a TX TLP Causes TLP Corruption	17-Nov-11	11.0		http://www.altera.com/support/kdb/solutions/spr382162.html
IP Compiler for PCI Express r2c_err0 Signal Toggles Unexpectedly	12-Oct-11	11.0	11.1	http://www.altera.com/support/kdb/solutions/spr389709.html
IP Compiler for PCI Express User Guide Does Not Document derr_cor_ext_rcv Signal as a Debug Signal	26-Oct-11	11.0		http://www.altera.com/support/kdb/solutions/spr385495.html
IP Compiler for PCI Express Root Port Bus Functional Model (BFM) and Endpoint Design Example Not Available	30-Sep-11	11.0 SP1		http://www.altera.com/support/kdb/solutions/spr381397.html
IP Compiler for PCI Express User Guide Does Not Include Pin Assignments in Qsys Design Example	30-Sep-11	11.0		http://www.altera.com/support/kdb/solutions/spr378471.html
IP Compiler for PCI Express Might Exceed Maximum ACK Latency When ASPM L0s is Enabled in Stratix IV Devices	16-Nov-11	10.0		http://www.altera.com/support/kdb/solutions/spr374837.html
IP Compiler for PCI Express Stratix IV GX Reset Controller Does Not Enter Recovery Immediately if Reference Clock Constraints are Not Met	30-Sep-11	11.0		http://www.altera.com/support/kdb/solutions/spr375834.html
SOPC Builder-Generated Hard IP Compiler for PCI Express Variations Might Violate FC Update Frequency Requirement	30-Sep-11	10.0		http://www.altera.com/support/kdb/solutions/spr376985.html
PCI Express User Guide Specifies Wrong Arria II GX Support for Avalon-MM 62.5 MHz Application Clock	15-Oct-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/spr372743.html
ModelSim-Altera Simulation of IP Compiler for PCI Express is Slow	10-Oct-11	11.0		http://www.altera.com/support/kdb/solutions/spr372961.html
PCI Express User Guide Incorrectly Shows Support for Avalon-MM Interface in Multiple Device Families	10-Oct-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/spr372971.html

Table 20–2. IP Compiler for PCI Express Errata Knowledge Base Links (Part 4 of 5)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
IP Compiler for PCI Express Qsys-Generated VHDL Testbench Cannot Simulate	10-Oct-11	11.0		http://www.altera.com/support/kdb/solutions/spr375688.html
PCI Express User Guide and Parameter Editor Allow Incorrect Application Clock Frequency for Stratix V GX Devices	10-Oct-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/spr368687.html
Hold Time Violations for IP Compiler for PCI Express Hard IP Variations on Arria II GZ Devices	10-Oct-11	10.1	11.0	http://www.altera.com/support/kdb/solutions/spr365679.html
IP Compiler for PCI Express Cannot Negotiate to Gen 2 Data Rate on Some Devices	10-Oct-11	10.0		http://www.altera.com/support/kdb/solutions/spr365541.html
Incorrect Arria II GZ Device Support in PCI Express Compiler User Guide	17-Nov-11	10.1	11.0	http://www.altera.com/support/kdb/solutions/spr363544.html
IP Compiler for PCI Express User Guide Incorrectly Includes an ALTGXB Reset Signal	10-Oct-11	10.1		http://www.altera.com/support/kdb/solutions/spr363651.html
Incorrect Numbering of 256-Bit Interface in PCI Express Compiler User Guide	10-Oct-11	10.1	11.0	http://www.altera.com/support/kdb/solutions/spr361724.html
PCI Express Compiler User Guide Does Not Clarify that Posted Requests and Completions May Be Blocked if rx_st_mask Is Asserted	10-Oct-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/spr360958.html
Incorrect Connections Shown in SOPC Builder Illustration in PCI Express Compiler User Guide	15-Nov-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/spr335915.html
Memory Read Requests Hang in the SOPC Builder Soft IP Implementation of the PCI Express Compiler	10-Oct-11	8.0	10.1 SP1	http://www.altera.com/support/kdb/solutions/spr362075.html
PCI Express Compiler Root Port Example Design Simulation Fails for Some Versions of ModelSim	10-Oct-11	10.0	10.1	http://www.altera.com/support/kdb/solutions/spr360639.html
VCS Simulation Script Fails for PCIe Root Port Design Example	10-Oct-11	8.0	10.1	http://www.altera.com/support/kdb/solutions/spr358971.html
SOPC Builder Hard IP Implementation of PCI Express Compiler Hangs when Entering L1 State	10-Oct-11	10.0	10.1	http://www.altera.com/support/kdb/solutions/spr356304.html

Table 20–2. IP Compiler for PCI Express Errata Knowledge Base Links (Part 5 of 5)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
The Transceiver May Be Incorrectly Reset in the PCI Express Compiler Leading to Unreliable PCI Express Link Behavior	17-Nov-11	10.0	10.1	http://www.altera.com/support/kdb/solutions/spr351111.html
Timing Analysis for PCI Express Compiler ×1 Variations That Target a Cyclone IV GX Device	17-Nov-11	10.0	10.1	http://www.altera.com/support/kdb/solutions/spr324113.html
PCI Express Compliance Test Does Not Generate Gen2 Compliance Pattern	10-Oct-11	10.0	10.1	http://www.altera.com/support/kdb/solutions/spr353170.html
IP Compiler for PCI Express Variations that Target an Arria II GX Device are Missing PLL_powerdown Signal when Using Custom Quartus II Installation	10-Oct-11	10.0		http://www.altera.com/support/kdb/solutions/spr349731.html
Compilation Fails for Hard IP PCI Express MegaCore Function in Stratix IV GT Devices	10-Oct-11	10.0	10.0 SP1	http://www.altera.com/support/kdb/solutions/spr350736.html
PCI Express Hard IP Compilation is Disabled for Gen1 ×4 and ×8 in Some Devices	17-Nov-11	10.0	10.0 SP1	http://www.altera.com/support/kdb/solutions/spr347615.html
PCI Express Design Example Does Not Always Close Timing in Stratix V GX and HardCopy IV GX Devices in 250 MHz Mode	10-Oct-11	10.0	10.0 SP1	http://www.altera.com/support/kdb/solutions/spr348291.html
MSI Requests not Supported in IP Compiler for PCI Express in Completer Only Mode	10-Oct-11	10.0		http://www.altera.com/support/kdb/solutions/spr335270.html
Incorrect <variation>_serdes.v(hd) File Produced When Editing an Older PCI Express Compiler Variation	10-Oct-11	9.1		http://www.altera.com/support/kdb/solutions/spr334127.html

Product Revision History

Table 21–1 shows the revision history for the NCO MegaCore function.

For information about the new features, refer to the *NCO MegaCore Function User Guide*.

Table 21–1. NCO MegaCore Function Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	Maintenance release.
11.0	May 2011	■ Final support for Arria II GX, Arria II GZ, Cyclone III LS, and Cyclone IV GX devices. ■ HardCopy Compilation support for HardCopy III, HardCopy IV E, and HardCopy IV GX devices.

Errata

For the most recent list of errata for the NCO MegaCore function, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the NCO MegaCore function.

22. Nios II Processor

For the most recent list of errata for the Nios® II processor core, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Product Revision History

Table 22–1 shows the revision history for the Nios II Processor MegaCore function.

For more information about the new features, refer to the *Nios II Processor Reference Handbook*. For information about new features and errata in the Nios II Embedded Design Suite, refer to the *Nios II Embedded Design Suite Release Notes and Errata*.

Table 22–1. Nios II Processor Revision History

Version	Date	Description
12.0	June 2012	Verified with the Quartus II software v12.0
11.1	November 2011	Verified with the Quartus II software v11.1
11.0	May 2011	Verified with the Quartus II software v11.0

Errata

☞ Not all issues affect all versions of the Nios II Processor.

Table 22–2.

Problem	Published Date	Version Found In	Version Fixed In	Knowledge Base Link
Nios II Processor Generates Incorrect Results from Shift Right (SRAI, SRA) Instructions	26-Jun-12	Version 11.0		http://www.altera.com/support/kdb/solutions/fb59094.html
Error Messages Shown when Nios II processor is Added in Qsys	22-Jun-12	Version 11.0		http://www.altera.com/support/kdb/solutions/fb52233.html
Qsys (Beta) might generate error messages for designs containing a Nios II processor	24-Oct-11	Version 10.1	Version 10.1	http://www.altera.com/support/kdb/solutions/spr358739.html
Error Running Nios II Project: 'Downloading ELF Process failed'	20-Sep-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr343469.html
Errors Adding Custom Instruction to the Nios II Processor	10-Sep-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr244264.html
Nios II Ports Created Incorrectly	17-Oct-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr246042.html
Simulation Fails for UniPHY External Memory Interfaces when Generating VHDL for Designs Using Nios II-based Sequencer	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr373105.html

23. PCI Compiler

Product Revision History

Table 23–1 shows the revision history for the PCI Compiler.

For more information about the new features, refer to the *PCI Compiler User Guide*.

Table 23–1. PCI Compiler Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	Maintenance release.
11.0	May 2011	Final support for Arria II GZ, Cyclone III LS, Cyclone IV E, and Cyclone IV GX device.

Errata

For the most recent list of errata for the PCI Compiler, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

The following sections addresses known errata and documentation issues for the PCI Compiler. Errata are functional defects or errors, which may cause the PCI Compiler to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Not all issues affect all versions of the PCI Compiler.

Table 23–2 lists the errata for this IP core, the relevant versions, and links to the Knowledge Base.

Table 23–2. Errata Knowledge Base Links

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Some PCI Compiler Designs With Cyclone III LS Devices Fail to Meet Timing	20-Jan-12	Version 10.0		http://www.altera.com/support/kdb/solutions/spr392323.html
Some PCI Compiler Designs With Stratix IV Devices Fail to Meet Timing	20-Jan-12	Version 10.0		http://www.altera.com/support/kdb/solutions/spr392327.html
Configuration Write to Invalid Address Repeats Continuosly	16-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr392322.html
F1152 Packages for HardCopy III and HardCopy IV E Not Supported	16-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr392324.html
Wirebond Packages for HardCopy III and HardCopy IV E Not Supported	16-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr392325.html

24. POS-PHY Level 4

Product Revision History

Table 24–1 shows the revision history for the POS-PHY Level 4 MegaCore function.

For more information about the new features, refer to the *POS-PHY Level 4 MegaCore Function User Guide*.

Table 24–1. POS-PHY Level 4 MegaCore Function Revision History

Date	Version	Description
June 2012	12.0	Verified with the Quartus II software v12.0.
November 2011	11.1	Verified with the Quartus II software v11.1.
May 2011	11.0	Verified with the Quartus II software v11.0.

Errata

For the most recent list of errata for the POS-PHY Level 4 MegaCore function, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

The following sections addresses known errata and documentation issues for the POS-PHY Level 4 MegaCore function. Errata are functional defects or errors, which may cause the POS-PHY Level 4 MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Not all issues affect all versions of the POS-PHY Level MegaCore function.

Table 24–2 lists the errata for this IP core, the relevant versions, and links to the Knowledge Base.

Table 24–2. Errata Knowledge Base Links (Part 1 of 2)

Issue	Date Last Modified	Version First Found	Version Fixed	Knowledge Base Link
VHDL IP Functional Simulation Fails	15-Jun-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr373389.html
POS-PHY Level 4 MegaCore Function Issues Irrelevant Signals: err_ry_msop* & err_ry_meop*	28-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr392819.html

Table 24–2. Errata Knowledge Base Links (Part 2 of 2)

Issue	Date Last Modified	Version First Found	Version Fixed	Knowledge Base Link
POS-PHY Level 4 MegaCore Function IP Toolbench Generation Fails if the Generation Is Cancelled and Restarted	28-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr392823.html
POS-PHY Level 4 MegaCore Function IP Toolbench Fails to Generate IP Functional Simulation Models for HardCopy Stratix Devices	28-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr392822.html
POS-PHY Level 4 MegaCore Function IP Toolbench has an Error After Changing the Device Family	28-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr392821.html
Incorrect LVDS Frequencies in Quartus II Compilation for the POS-PHY Level 4 MegaCore Function	28-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr392818.html
POS-PHY Level 4 MegaCore Function Issues Warning Message: Pin “err_rd_dpa” Stuck at GND	28-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr392820.html
Import PLL Frequency Launches Incorrect Parameter Editor	26-Sep-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr358920.html
Cannot Edit ALTPLL Megafunction for Stratix V Devices	26-Sep-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr352626.html
Training Interval is Greater than Specified	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr243211.html
Errors when Editing Transmitters v7.2 or Earlier in v8.0	23-Aug-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr274695.html

25. QDRII SRAM

Product Revision History

Table 25–1 shows the revision history for the QDRII SRAM MegaCore function.

For more information about the new features, refer to the *QDRII SRAM MegaCore Function User Guide*.

Table 25–1. QDRII SRAM MegaCore Function Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	Maintenance release.
11.0	May 2011	Maintenance release.

Errata

For the most recent list of errata for the QDRII SRAM MegaCore function, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

26. QDR II and QDR II+ SRAM Controller with UniPHY

Product Revision History

Table 26–1 shows the revision history for the QDR II and QDR II+ SRAM Controller with UniPHY.

For more information about the new features, refer to the *External Memory Interface Handbook*.

Table 26–1. QDR II and QDR II+ SRAM Controller with UniPHY Revision History

Version	Date	Description
12.0	June 2012	Added new EMIF Toolkit
11.1 SP2	February 2012	Added EMIF Toolkit support for Stratix V
11.1	November 2011	Added support for Arria V devices
11.0 SP1	July 2011	Verified with the Quartus II software v11.0 SP1
11.0	May 2011	■ Added Nios II-based sequencer ■ Upgraded f_{MAX} (with Nios II sequencer) to 550 MHz for Stratix III, Stratix IV, and Stratix V devices

Errata

For the most recent list of errata for the QDR II and QDR II+ SRAM Controller with UniPHY IP core, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

The following sections addresses known errata and documentation issues for the QDR II and QDR II+ SRAM Controller with UniPHY IP core. Errata are functional defects or errors, which may cause the QDR II and QDR II+ SRAM Controller with UniPHY IP core to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Not all issues affect all versions of the QDR II and QDR II+ SRAM Controller with UniPHY IP core.

Table 26–2 lists the errata for this IP core, the relevant versions, and a link to the Knowledge Base.

Table 26–2. Errata Knowledge Base Links (Part 1 of 6)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Designs Targeting Stratix V ES Devices May Fail Timing in TimeQuest	14-Feb-12	Version 11.1 SP2	Version 12.0	http://www.altera.com/support/kdb/solutions/spr394081.html
NativeLink Simulation in UniPHY External Memory Interfaces fail for VHDL Output	18-Nov-11	Version 10.0	Version 12.0	http://www.altera.com/support/kdb/solutions/spr362558.html
Cannot Share One PLL/DLL/OCT Master with Multiple Slaves in Qsys for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 12.0	http://www.altera.com/support/kdb/solutions/spr372587.html
NativeLink Simulation for UniPHY External Memory Interfaces fails for VHDL Output	18-Nov-11	Version 10.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr362559.html
Simulation with NC Sim or Riviera-PRO Fails with an Elaboration Error for UniPHY External Memory Interfaces	18-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr377595.html
VHDL-Generated Fileset Can Encounter Synthesis Problems for UniPHY External Memory Interfaces	18-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr377804.html
Warning Messages About afi_rdata_valid, afi_rdata_en, afi_rdata_en_full	15-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr388691.html
Unexpected Timing Results in Design With Both ALTMEMPHY and UniPHY	15-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr390608.html
Selecting VHDL for QDR II and QDR II+ SRAM Controller with UniPHY or RLDRAM II Controller with UniPHY Gives a Verilog HDL IP Core	23-Nov-11	Version 10.0	Version 12.0	http://www.altera.com/support/kdb/solutions/spr349629.html
Clock mem_cq_n Not Used for QDR Interfaces on Arria V and Cyclone V	15-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr387780.html
SOPC Builder Issues Erroneous Error Message	15-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr387451.html
UniPHY EMIF Toolkit Reports Narrow Data Valid Window	15-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr387075.html
Calibration May Fail Without Issuing CAL_FAIL Signal	14-Feb-12	Version 11.1 SP2	Version 12.0	http://www.altera.com/support/kdb/solutions/spr394052.html
For V-series Families, VHDL is Not Supported When Read DQS Tracking is Enabled	14-Feb-12	Version 11.1 SP1	Version 11.1 SP2	http://www.altera.com/support/kdb/solutions/spr392499.html

Table 26–2. Errata Knowledge Base Links (Part 2 of 6)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Fitter Error Occurs When Read DQS Tracking is Enabled	14-Feb-12	Version 11.1 SP1	Version 11.1 SP2	http://www.altera.com/support/kdb/solutions/spr392718.html
Calibration Fails for QDR II/II+ Designs Targeting Stratix V Devices	15-Nov-11	Version 11.1	Version 11.1 SP2	http://www.altera.com/support/kdb/solutions/spr391166.html
Timing-Related Warning Messages for QDR II and QDR II+ SRAM Controller with UniPHY and RLDRAM II Controller with UniPHY When Sharing PLLs on Stratix V Devices	23-Nov-11	Version 10.1	Version 11.1	http://www.altera.com/support/kdb/solutions/spr361404.html
Simulation Fails for UniPHY External Memory Interfaces with “Undefined System Task Call” Error	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr373731.html
Example Design Simulation for UniPHY External Memory Interfaces May Fail in NC Sim	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr371331.html
Simulation Fails for UniPHY External Memory Interfaces when Generating VHDL for Designs Using Nios II-based Sequencer	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr373105.html
PLL Master Required for Simulation of PLL Slave for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr374852.html
Conduit Error Messages Displayed in Qsys for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr372446.html
Simulation of Example Designs Can Fail or Produce Warnings for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr368146.html
Write Timing Violation at 550MHz for QDR II and QDR II+ SRAM Controller with UniPHY	23-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr374201.html
Stratix V QDR II and QDR II+ SRAM Controller with UniPHY and RLDRAM II Controller with UniPHY Memory Interfaces May Exhibit Write Timing Failure	23-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr376564.html
UniPHY CSR Ports Not Functioning Correctly for External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr377353.html

Table 26–2. Errata Knowledge Base Links (Part 3 of 6)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Example Project Fails to Simulate When HardCopy Compatibility is Enabled for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr375477.html
ModelSim Waveform Viewer for UniPHY External Memory Interfaces Shows Only clk and reset Signals	18-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr375193.html
Minimum Pulse Width Timing Failures for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr374717.html
Calibration Failure for QDR II and QDR II+ SRAM Controller with UniPHY and RLDRAM II Controller with UniPHY in Earlier Versions	23-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr357211.html
VHDL-Only Simulation Not Supported for QDR II and QDR II+ SRAM Controller with UniPHY and RLDRAM II Controller with UniPHY	23-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr364154.html
QDR II and QDR II+ SRAM Controller with UniPHY IP Core May Not Operate Below 167MHz	23-Nov-11	Version 10.0	Version 11.0	http://www.altera.com/support/kdb/solutions/spr344828.html
Incorrect Clock Uncertainty in UniPHY External Memory Interfaces	18-Nov-11	Version 10.0	Version 11.0	http://www.altera.com/support/kdb/solutions/spr344172.html
Example Designs for UniPHY External Memory Interfaces May Not Compile for IP Cores from Earlier Versions	18-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr357422.html
SOPC Builder-generated Systems Cannot Serve as Top-Level Design for UniPHY External Memory Interfaces	18-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr356433.html
Compilation Fails for UniPHY External Memory Interfaces if Synthesis Fileset is Mixed with Example Project Files	18-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr359597.html
Warning Messages Displayed for UniPHY External Memory Interfaces When Compiling for Stratix V Devices	18-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr358219.html
BSF File Not Generated for UniPHY External Memory Interfaces	23-Nov-11	Version 10.0	Version 10.1	http://www.altera.com/support/kdb/solutions/spr346650.html

Table 26–2. Errata Knowledge Base Links (Part 4 of 6)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Simulation Error QDR II and QDR II+ SRAM Controller with UniPHY	23-Nov-11	Version 10.0	Version 10.0 SP1	http://www.altera.com/support/kdb/solutions/spr345850.html
Center PLL in Arria V Cannot Drive Two Independent PHY Clock Networks	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb60761.html
VHDL Post-Fit Simulation Failure on Stratix V Devices	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb56374.html
EMIF Toolkit Will Not Link to Designs Created in Qsys	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb55124.html
PHY Clock Tree Not Driven by Optimal PLL Output Counters	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb55089.html
Arria V and Cyclone V Hard Memory Controller Options May Not Function Correctly for Interfaces with 2 Chip Selects	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb53386.html
Warning Messages Displayed in TimeQuest	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb51089.html
Possible Internal Error with Arria V or Cyclone V Designs Using Hard Memory Controller	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb49167.html
EMIF Toolkit Will Not Link to Projects Containing In-System Memory Editor	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb48648.html
Altera QDR II Memory Model Behaves Differently Than Other Vendors' Memory Models During Concurrent Transactions	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb48625.html
Simulation Example Design Fails and Produces Warnings	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb44572.html
Memory IP on Stratix V Devices Does Not Support Frequencies Below 150 MHz	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb41666.html
Calibration Failure Occurs when RELEASE_CLEARS_BEFORE_TRI_STATES is On	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb40520.html
Example Design for Arria V with Hard Memory Interface Uses Wrong Clock	14-Feb-12	Version 11.1		http://www.altera.com/support/kdb/solutions/fb31983.html
User Refresh Limitation in Arria V and Cyclone V Hard Memory Interface	14-Feb-12	Version 11.1		http://www.altera.com/support/kdb/solutions/fb31428.html

Table 26–2. Errata Knowledge Base Links (Part 5 of 6)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Incorrect IP Functional Simulation Model for QDR II and QDR II+ SRAM Controller with UniPHY	23-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr326301.html
Global Signal Assignments for UniPHY External Memory Interfaces Not Applied	23-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr345461.html
Simulation Fails with PLL Clocks Out of Synchronization for UniPHY External Memory Interfaces	23-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr352405.html
Example Design Can Fail For Certain Parameterizations of QDR II and QDR II+ SRAM Controller with UniPHY and DDR2 and DDR3 SDRAM Controller with UniPHY	23-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr371214.html
DQS Clock Buffer Location for QDR II and QDR II+ SRAM Controller with UniPHY and RLDRAM II Controller with UniPHY	23-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr324219.html
No Link to the External Memory Interface Handbook from Wizard	23-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr324773.html
Error Messages for UniPHY External Memory Interfaces in ModelSim Flow for Eclipse	18-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr375252.html
Cannot Launch MegaWizard Plug-In Manager by Opening Example Design for UniPHY External Memory Interfaces	18-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr357643.html
Higher Delays and Skews Expected for UniPHY External Memory Interfaces Corner I/Os in Stratix V Devices	18-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr351007.html
UniPHY IP Generation for External Memory Interfaces Fails if the Quartus II Installation Path Contains a Space	18-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr376172.html
Unable to Directly Recompile Quartus II version 10.1 Design for UniPHY External Memory Interfaces in Quartus II version 11.0	18-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr373335.html

Table 26–2. Errata Knowledge Base Links (Part 6 of 6)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Compilation of a UniPHY Example Design Can Produce Warnings for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr367353.html
How to Use UniPHY-based Memory IP with SOPC Builder	18-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr373304.html
Reset Synchronizer for UniPHY External Memory Interfaces May Cause Design to Fail Timing when generated in SOPC Builder or Qsys	18-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr360104.html
Erroneous Timing Failures in Designs Containing Both UniPHY and ALTMEMPHY Instantiations for External Memory Interfaces	18-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr377893.html
Segmentation Fault During Elaboration with ModelSim SE	15-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr392043.html
VCS-MX Simulation with Simulation Script vcsmx_setup.sh Fails at 0ns	15-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr388472.html
Error Occurs When Running Simulation Example Design in ModelSim	15-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr387730.html
Full-rate QDR II and RLDRAM II Are Not Supported for Arria V	15-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr390872.html

Product Revision History

Table 27–1 shows the revision history for the RapidIO MegaCore function.

For more information about the new features, refer to the *RapidIO MegaCore Function User Guide*.

Table 27–1. RapidIO MegaCore Function Revision History

Version	Date	Description
12.0	June 2012	■ Added support for Cyclone V GT x1 variation at 5.0 Gbaud.
11.1	November 2011	■ Preliminary support for Arria V and Cyclone V device. ■ Support for Custom PHY IP core in variations that target an Arria V or Cyclone V device
11.0	May 2011	■ Preliminary support for Stratix V devices ■ Support for Custom PHY IP core in variations that target a Stratix V device ■ Final support for Arria II GZ, Cyclone III LS, and Cyclone IV GX devices ■ HardCopy Compilation support for HardCopy III, HardCopy IV E, and HardCopy IV GX devices

Errata

For the most recent list of errata for the RapidIO MegaCore function, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the RapidIO MegaCore function. Altera recommends upgrading to the latest available version of the MegaCore IP Library.

Table 27–2 lists the errata for the RapidIO MegaCore function, the relevant software releases, and links to the Knowledge Base.

Table 27–2. RapidIO MegaCore Function Errata Knowledge Base Links (Part 1 of 3)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
Wrong Default Transceiver Equalization Setting in RapidIO IP Core in Some Device Families	28-Jun-12	9.1		http://www.altera.com/support/kdb/solutions/fb52169.html
Qsys-Generated RapidIO IP Core Does Not Generate .pof Through Open Core Plus Program	28-Jun-12	10.1	12.0	http://www.altera.com/support/kdb/solutions/fb36354.html

Table 27–2. RapidIO MegaCore Function Errata Knowledge Base Links (Part 2 of 3)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
Generation of RapidIO MegaCore Function Stalls in Arria GX and Stratix II GX Designs	30-Jan-12	10.0		http://www.altera.com/support/kdb/solutions/spr339172.html
RapidIO IP Core VHDL Customer Testbench Fails Simulation For Some Arria V Variations	28-Jun-12	11.1	12.0	http://www.altera.com/support/kdb/solutions/spr392010.html
Potential for Loss of Order between Read and Write Transactions in RapidIO I/O Avalon-MM Master	13-Dec-11	11.0		http://www.altera.com/support/kdb/solutions/spr389007.html
Cannot Export Some Interfaces in Qsys-Generated RapidIO IP Core	20-Nov-11	11.1		http://www.altera.com/support/kdb/solutions/spr392585.html
RapidIO IP Core Customer Testbench Fails Simulation For Some Arria V Variations With Mismatched Reference Clock Frequency	28-Jun-12	11.1	11.1 SP2	http://www.altera.com/support/kdb/solutions/spr391943.html
Qsys-Generated RapidIO IP Core Appears to Allow Larger Revision IDs Than are Implemented	20-Nov-11	10.1	11.0	http://www.altera.com/support/kdb/solutions/spr357833.html
Ignored set_false_path and Ignored filter Warnings for RapidIO Variations That Target an Arria V, Cyclone V, or Stratix V Device	27-Sep-11	11.0		http://www.altera.com/support/kdb/solutions/spr376485.html
Cannot Simulate Qsys-Generated RapidIO IP Core Testbench VHDL Model	20-Nov-11	11.0	11.1	http://www.altera.com/support/kdb/solutions/spr375076.html
Warning Message Indicates RapidIO IP Core Preliminary Support for Cyclone IV GX Devices	27-Sep-11	11.0	11.0 SP1	http://www.altera.com/support/kdb/solutions/spr374898.html
RapidIO MegaCore Function Transport Layer Receive Buffer Can Overflow	27-Sep-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/spr368962.html
RapidIO MegaCore Function User Guide Does Not Clarify that Migration from SOPC Builder to Qsys Changes Port Names	27-Sep-11	10.1	11.0	http://www.altera.com/support/kdb/solutions/spr356700.html
RapidIO IP Core Device and Assembly Register Values Might Lose MSBs	27-Sep-11	10.1	11.0	http://www.altera.com/support/kdb/solutions/spr360350.html
Certain Changes Made in the RapidIO Parameter Editor are Ignored	27-Sep-11	9.1 SP1	11.0	http://www.altera.com/support/kdb/solutions/spr335362.html
Changes Made to the RapidIO IP Core Transceiver Reference Clock in the ALTGX Parameter Editor are Ignored	20-Nov-11	9.1	11.0	http://www.altera.com/support/kdb/solutions/spr324301.html

Table 27–2. RapidIO MegaCore Function Errata Knowledge Base Links (Part 3 of 3)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
Warning Message Indicates RapidIO IP Core Preliminary Support for Arria II GX Devices	20-Nov-11	10.1	10.1 SP1	http://www.altera.com/support/kdb/solutions/spr359663.html
RapidIO Parameter Values Modified in SOPC to Qsys Conversion	27-Sep-11	10.1	10.1 SP1	http://www.altera.com/support/kdb/solutions/spr360425.html
Cannot Regenerate RapidIO MegaCore Function with Read-Only .qip File	27-Sep-11	10.0		http://www.altera.com/support/kdb/solutions/spr363643.html
Some RapidIO MegaCore Function Variations Return Incorrect Read Data	20-Nov-11	10.0	10.1	http://www.altera.com/support/kdb/solutions/spr357495.html
Some Cyclone III RapidIO Designs Fail Hold Time Requirements in TimeQuest Timing Analyzer	27-Sep-11	10.0	10.1	http://www.altera.com/support/kdb/solutions/spr347647.html
Migrated RapidIO Designs Automatically Set to Seven link-request Attempts	27-Sep-11	10.0	10.0 SP1	http://www.altera.com/support/kdb/solutions/spr350743.html
Stratix II GX Transceiver Transmitter Buffer Power Does Not Regenerate Correctly in a RapidIO IP Core	27-Sep-11	10.0	10.0 SP1	http://www.altera.com/support/kdb/solutions/spr347650.html
Unsupported Input Clock Frequencies Available in RapidIO Parameter Editor	27-Sep-11	10.0	10.0 SP1	http://www.altera.com/support/kdb/solutions/spr347651.html
RapidIO Parameter Editor Does Not Warn That Small Cyclone IV GX Devices Are Not Supported	27-Sep-11	10.0		http://www.altera.com/support/kdb/solutions/spr349846.html
The Demonstration Testbench May Fail for Some RapidIO Variations	27-Sep-11	10.0		http://www.altera.com/support/kdb/solutions/spr345734.html
Incorrect cmu_pll_inclock_period in Stratix II GX and Arria GX Designs	27-Sep-11	10.0		http://www.altera.com/support/kdb/solutions/spr347648.html
Critical Warning Displays if RapidIO IP Core System Clock and Reference Clock Have Same Source	20-Nov-11	10.0		http://www.altera.com/support/kdb/solutions/spr338966.html
Some RapidIO Variations With High Reference Clock Frequency Generate Critical Timing Warnings	27-Sep-11	9.0 SP2		http://www.altera.com/support/kdb/solutions/spr323092.html

28. Reed-Solomon Compiler

Product Revision History

Table 28–1 shows the revision history for the Reed-Solomon Compiler.

For more information about the new features, refer to the *Reed-Solomon Compiler User Guide*.

Table 28–1. Reed-Solomon Compiler Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	Maintenance release.
11.0	May 2011	■ Final support for Arria II GX, Arria II GZ, Cyclone III LS, and Cyclone IV GX devices. ■ HardCopy Compilation support for HardCopy III, HardCopy IV E, and HardCopy IV GX devices.

Errata

For the most recent list of errata for the Reed-Solomon Compiler, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the Reed-Solomon Compiler.

29. Reed-Solomon II

Product Revision History

Table 29–1 shows the revision history for Reed-Solomon II.

For information about the new features, refer to the *Reed-Solomon II MegaCore Function User Guide*.

Table 29–1. Reed-Solomon II Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	Maintenance release.
11.0	May 2011	Added new status ports and timing diagrams.

Errata

For the most recent list of errata for the Reed-Solomon II, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the Reed-Solomon II.

30. RLDRAM II

Revision History

Table 30–1 shows the revision history for the RLDRAM II MegaCore function.

For more information about the new features, refer to the *RLDRAM II MegaCore Function User Guide*.

Table 30–1. RLDRAM II MegaCore Function Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	Maintenance release.
11.0	May 2011	Maintenance release.

Errata

For the most recent list of errata for the RLDRAM II MegaCore function, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

31. RLDRAM II Controller with UniPHY

Product Revision History

Table 31–1 shows the revision history for the RLDRAM II Controller with UniPHY.

For more information about the new features, refer to the *External Memory Interface Handbook.*

Table 31–1. RLDRAM II Controller with UniPHY Revision History

Version	Date	Description
12.0	June 2012	Added new EMIF Toolkit
11.1 SP2	February 2012	Added EMIF Toolkit support for Stratix V
11.1	November 2011	Added support for Arria V devices
11.0 SP1	July 2011	Verified with the Quartus II software v11.0 SP1
11.0	May 2011	■ Added Nios II-based sequencer ■ Upgraded f_{MAX} (with Nios II sequencer): ■ To 533 MHz for Stratix III, Stratix IV, and Stratix V devices ■ To 400 MHz for HardCopy IV devces

Errata

For the most recent list of errata for the RLDRAM II Controller with UniPHY IP core, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

The following sections addresses known errata and documentation issues for the RLDRAM II Controller with UniPHY IP core. Errata are functional defects or errors, which may cause the RLDRAM II Controller with UniPHY IP core to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Not all issues affect all versions of the RLDRAM II Controller with UniPHY IP core.

Table 31–2 lists the errata for this IP core, the relevant versions, and a link to the Knowledge Base.

Table 31–2. Errata Knowledge Base Links (Part 1 of 6)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
NativeLink Simulation in UniPHY External Memory Interfaces fail for VHDL Output	18-Nov-11	Version 10.0	Version 12.0	http://www.altera.com/support/kdb/solutions/spr362558.html
Cannot Share One PLL/DLL/OCT Master with Multiple Slaves in Qsys for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 12.0	http://www.altera.com/support/kdb/solutions/spr372587.html
NativeLink Simulation for UniPHY External Memory Interfaces fails for VHDL Output	18-Nov-11	Version 10.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr362559.html
Simulation with NC Sim or Riviera-PRO Fails with an Elaboration Error for UniPHY External Memory Interfaces	18-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr377595.html
VHDL-Generated Fileset Can Encounter Synthesis Problems for UniPHY External Memory Interfaces	18-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr377804.html
Warning Messages About afi_rdata_valid, afi_rdata_en, afi_rdata_en_full	15-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr388691.html
Selecting VHDL for QDR II and QDR II+ SRAM Controller with UniPHY or RLDRAM II Controller with UniPHY Gives a Verilog HDL IP Core	23-Nov-11	Version 10.0	Version 12.0	http://www.altera.com/support/kdb/solutions/spr349629.html
SOPC Builder Issues Erroneous Error Message	15-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr387451.html
For V-series Families, VHDL is Not Supported When Read DQS Tracking is Enabled	14-Feb-12	Version 11.1 SP1	Version 11.1 SP2	http://www.altera.com/support/kdb/solutions/spr392499.html
Fitter Error Occurs When Read DQS Tracking is Enabled	14-Feb-12	Version 11.1 SP1	Version 11.1 SP2	http://www.altera.com/support/kdb/solutions/spr392718.html
UniPHY EMIF Toolkit Reports Narrow Data Valid Window	15-Nov-11	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr387075.html
Efficiency Monitor Latency Values Are Incorrect for DDR2 and DDR3 SDRAM Controller with UniPHY and RLDRAM II Controller with UniPHY	23-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr376056.html

Table 31–2. Errata Knowledge Base Links (Part 2 of 6)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Must Enable Support for Nios II ModelSim Flow in GUI for DDR2 and DDR3 SDRAM Controller with UniPHY and RLDRAM II Controller with UniPHY	23-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr371218.html
Timing-Related Warning Messages for QDR II and QDR II+ SRAM Controller with UniPHY and RLDRAM II Controller with UniPHY When Sharing PLLs on Stratix V Devices	23-Nov-11	Version 10.1	Version 11.1	http://www.altera.com/support/kdb/solutions/spr361404.html
Simulation Fails for UniPHY External Memory Interfaces with “Undefined System Task Call” Error	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr373731.html
Example Design Simulation for UniPHY External Memory Interfaces May Fail in NC Sim	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr371331.html
Simulation Fails for UniPHY External Memory Interfaces when Generating VHDL for Designs Using Nios II-based Sequencer	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr373105.html
PLL Master Required for Simulation of PLL Slave for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr374852.html
Conduit Error Messages Displayed in Qsys for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr372446.html
Simulation of Example Designs Can Fail or Produce Warnings for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr368146.html
RLDRAM II Controller with UniPHY Simulation fails in Riviera-PRO	24-Nov-11	Version 11.0 SP1	Version 11.0 SP2	http://www.altera.com/support/kdb/solutions/spr379362.html
Stratix V QDR II and QDR II+ SRAM Controller with UniPHY and RLDRAM II Controller with UniPHY Memory Interfaces May Exhibit Write Timing Failure	23-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr376564.html
UniPHY CSR Ports Not Functioning Correctly for External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr377353.html

Table 31–2. Errata Knowledge Base Links (Part 3 of 6)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Example Project Fails to Simulate When HardCopy Compatibility is Enabled for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr375477.html
ModelSim Waveform Viewer for UniPHY External Memory Interfaces Shows Only clk and reset Signals	18-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr375193.html
Minimum Pulse Width Timing Failures for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr374717.html
–18 Presets Give Errors for RLDRAM II Controller with UniPHY	24-Nov-11	Version 10.0	Version 11.0	http://www.altera.com/support/kdb/solutions/spr326182.html
Calibration Failure for QDR II and QDR II+ SRAM Controller with UniPHY and RLDRAM II Controller with UniPHY in Earlier Versions	23-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr357211.html
VHDL-Only Simulation Not Supported for QDR II and QDR II+ SRAM Controller with UniPHY and RLDRAM II Controller with UniPHY	23-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr364154.html
Incorrect Clock Uncertainty in UniPHY External Memory Interfaces	18-Nov-11	Version 10.0	Version 11.0	http://www.altera.com/support/kdb/solutions/spr344172.html
Example Designs for UniPHY External Memory Interfaces May Not Compile for IP Cores from Earlier Versions	18-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr357422.html
SOPC Builder-generated Systems Cannot Serve as Top-Level Design for UniPHY External Memory Interfaces	18-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr356433.html
Compilation Fails for UniPHY External Memory Interfaces if Synthesis Fileset is Mixed with Example Project Files	18-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr359597.html
Warning Messages Displayed for UniPHY External Memory Interfaces When Compiling for Stratix V Devices	18-Nov-11	Version 10.1	Version 11.0	http://www.altera.com/support/kdb/solutions/spr358219.html
BSF File Not Generated for UniPHY External Memory Interfaces	23-Nov-11	Version 10.0	Version 10.1	http://www.altera.com/support/kdb/solutions/spr346650.html

Table 31–2. Errata Knowledge Base Links (Part 4 of 6)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Center PLL in Arria V Cannot Drive Two Independent PHY Clock Networks	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb60761.html
VHDL Post-Fit Simulation Failure on Stratix V Devices	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb56374.html
EMIF Toolkit Will Not Link to Designs Created in Qsys	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb55124.html
PHY Clock Tree Not Driven by Optimal PLL Output Counters	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb55089.html
Arria V and Cyclone V Hard Memory Controller Options May Not Function Correctly for Interfaces with 2 Chip Selects	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb53386.html
Warning Messages Displayed in TimeQuest	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb51089.html
Possible Internal Error with Arria V or Cyclone V Designs Using Hard Memory Controller	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb49167.html
EMIF Toolkit Will Not Link to Projects Containing In-System Memory Editor	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb48648.html
Simulation Example Design Fails and Produces Warnings	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb44572.html
Calibration Failure Occurs when RELEASE_CLEARS_BEFORE_TRI_STATES is On	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb40520.html
User Refresh Limitation in Arria V and Cyclone V Hard Memory Interface	01-Jul-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb31428.html
User Refresh Limitation in Arria V and Cyclone V Hard Memory Interface	14-Feb-12	Version 11.1		http://www.altera.com/support/kdb/solutions/fb31428.html
Enable Avalon-MM Byte-Enable Signal Option Not Functional for RLDRAM II Controller with UniPHY	24-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr375643.html
Efficiency Monitor Statistics Incorrect for Initial Sample in DDR2 and DDR3 SDRAM Controller with UniPHY and RLDRAM II Controller with UniPHY	23-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr374202.html
Global Signal Assignments for UniPHY External Memory Interfaces Not Applied	23-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr345461.html

Table 31–2. Errata Knowledge Base Links (Part 5 of 6)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Simulation Fails with PLL Clocks Out of Synchronization for UniPHY External Memory Interfaces	23-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr352405.html
DQS Clock Buffer Location for QDR II and QDR II+ SRAM Controller with UniPHY and RLDRAM II Controller with UniPHY	23-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr324219.html
No Link to the External Memory Interface Handbook from Wizard	23-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr324773.html
Error Messages for UniPHY External Memory Interfaces in ModelSim Flow for Eclipse	18-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr375252.html
Cannot Launch MegaWizard Plug-In Manager by Opening Example Design for UniPHY External Memory Interfaces	18-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr357643.html
Higher Delays and Skews Expected for UniPHY External Memory Interfaces Corner I/Os in Stratix V Devices	18-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr351007.html
UniPHY IP Generation for External Memory Interfaces Fails if the Quartus II Installation Path Contains a Space	18-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr376172.html
Unable to Directly Recompile Quartus II version 10.1 Design for UniPHY External Memory Interfaces in Quartus II version 11.0	18-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr373335.html
Compilation of a UniPHY Example Design Can Produce Warnings for UniPHY External Memory Interfaces	18-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr367353.html
How to Use UniPHY-based Memory IP with SOPC Builder	18-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr373304.html
Reset Synchronizer for UniPHY External Memory Interfaces May Cause Design to Fail Timing when generated in SOPC Builder or Qsys	18-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr360104.html

Table 31–2. Errata Knowledge Base Links (Part 6 of 6)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Erroneous Timing Failures in Designs Containing Both UniPHY and ALTMEMPHY Instantiations for External Memory Interfaces	18-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr377893.html
Segmentation Fault During Elaboration with ModelSim SE	15-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr392043.html
VCS-MX Simulation with Simulation Script vcsmx_setup.sh Fails at 0ns	15-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr388472.html
Error Occurs When Running Simulation Example Design in ModelSim	15-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr387730.html
Full-rate QDR II and RLDRAM II Are Not Supported for Arria V	15-Nov-11	Version 11.1		http://www.altera.com/support/kdb/solutions/spr390872.html

Product Revision History

Table 32–1 shows the revision history for the SDI MegaCore function.

For more information about the new features, refer to the *SDI MegaCore Function User Guide*.

Table 32–1. SDI MegaCore Function Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	■ Preliminary support for Arria V devices. ■ Added new optional transmitter feature: Transmitter clock multiplexer.
11.0	May 2011	■ Preliminary support for Stratix V devices. ■ Final support for Arria II GZ, Cyclone III LS, and Cyclone IV GX devices. ■ Added new 8-bit video format output features for receiver and duplex instances. ■ Added unencrypted ALTGX wrapper file. ■ Added incoming video data rate indicator. ■ Removed Enable Spread Spectrum feature.

Errata

For the most recent list of errata for the SDI MegaCore function, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the SDI MegaCore function.

33. SerialLite II

Product Revision History

Table 33–1 shows the revision history for the SerialLite II MegaCore function.

For more information about the new features, refer to the *SerialLite II MegaCore Function User Guide*.

Table 33–1. SerialLite II MegaCore Function Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	Maintenance release.
11.0	May 2011	Maintenance release.

Errata

For the most recent list of errata for the SerialLite II MegaCore function, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the SerialLite II MegaCore function.

34. Stratix V Hard IP for PCI Express

Product Revision History

Table 34–1 shows the revision history for the Stratix V Hard IP for PCI Express.

For more information about the new features, refer to the *Stratix V Hard IP for PCI Express User Guide*.

Table 34–1. Stratix V Hard IP for PCI Express Revision History

Date	Version	Description
July 2012	12.0	Added the following new features: ■ Avalon-MM single dword variant. ■ Programmer Object File (**.pof**) support for Stratix V devices. ■ Gen3 ×1 and ×4 support for Avalon-MM Endpoints. ■ C4 speed grade for all variants except Gen3 ×8 and Gen3 ×4 with 128-bit interface. ■ C1 speed grade is available for all variants.
February 2012	11.1 SP2	Verified with the Quartus II software v11.1 SP2.
December 2011	11.1 SP1	Verified with the Quartus II software v11.1 SP1.
November	11.1	Added the following new features: ■ Support for x1, x4, and x8 Gen3 variants with the Avalon-ST interface ■ Support for x1, x4, and x8 Gen1 and Gen2 variants with the Avalon-MM interface ■ Support for multiple packets per cycle when using the 256-bit interface ■ Added **.pof** support for Stratix V ES devices for Gen1 and Gen2
July 2011	11.0 SP1	Verified with the Quartus II software v11.0 SP1.
May 2011	11.0	First release

Errata

For a recent list of errata and affected versions of the Stratix V Hard IP for PCI Express IP core, refer to the Altera **Knowledge Base** page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the Stratix V Hard IP for PCI Express.

Table 34–2 lists the errata for the Hard IP for PCI Express, the relevant software releases, and links to the Knowledge Base.

Table 34–2. Hard IP for PCI Express Errata Knowledge Base Links (Part 1 of 3)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Stratix V Avalon-MM Hard IP for PCI Express IP Core Testbench Generation Fails	7-Feb-12	Version 11.1 SP2	Version 12.0	http://www.altera.com/support/kdb/solutions/fb35231.html
Clock Connections for the Stratix V Hard IP when Using CvP with Additional Transceiver PHY IP Cores	9-Jan-12	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr388445.html
Definition of fixedclk Incorrect for PHY IP Core for PCI Express (PIPE)	9-Jan-12	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/spr393795.html
Incorrect Definition of npor Reset in the Stratix V Hard IP for PCI Express User Guide	8-Feb-12	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/fb37883.html
Stratix V Hard IP for PCI Express Simulation Incorrectly Retransmitting TLPs	8-Feb-12	Version 11.1	Version 12.0	http://www.altera.com/support/kdb/solutions/fb36596.html
Hard IP for PCI Express User Guides Shows Incorrect Value for Receiver Detect Capacitor	03-July-12	Version 12.0		http://www.assmltera.com/support/kdb/solutions/fb61602.html
Stratix V Hard IP for PCI Express User Guide Shows Incorrect Channel Placement for CMU PLL	03-July-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb61670.html
Excessive Warnings in the VHDL Design Example for Stratix V Hard IP for PCI Express IP Core	12-June-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb46686.html
Stratix V Hard IP for PCI Express IP Core Fails To Log First Error Pointer for Completion Timeout Error	12-June-12	Version 10.1		http://www.altera.com/support/kdb/solutions/fb50477.html

Table 34–2. Hard IP for PCI Express Errata Knowledge Base Links (Part 2 of 3)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Stratix V Hard IP for PCI Express IP Core Gen3 x8 app_rstn Timing Issue	12-June-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb49184.html
C4 Speed Grade Should Be Available for Gen2 Variants of the Stratix V Hard IP for PCI Express IP Core	08-June-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb50844.html
reconfig_xcvr_clk Hold Time Failure for Gen1 x1 Variants of the Stratix V Hard IP for PCI Express IP Core Variants	08-June-12	Version 12.0		http://www.altera.com/support/kdb/solutions/fb49125.html
MSI-X Not Working Correctly in the Stratix V Hard IP for PCI Express IP Core	8-Feb-12	Version 11.0	Version 11.1 SP2	http://www.altera.com/support/kdb/solutions/spr393499.html
Stratix V Hard IP for PCI Express Root Port Includes Unsupported Interrupt Signals	8-Feb-12	Version 10.1	Version 11.1 SP2	http://www.altera.com/support/kdb/solutions/spr392896.html
Top-Level Stratix V PCI Express Module Includes derr_cor_ext_rcv1	9-Nov-11	Version 11.0	Version 11.0 SP1	http://www.altera.com/support/kdb/solutions/spr375931.html
Compliance Base Board (CBB) Testing Fails for Stratix V Hard IP for PCI Express	9-Nov-11	Version 11.0	Version 11.1 SP1	http://www.altera.com/support/kdb/solutions/spr390420.html
Error in Getting Started Instructions for Post-Compilation Simulation	8-Nov-11	Version 11.0	Version 11.1	http://www.altera.com/support/kdb/solutions/spr376054.html
Stratix V Hard IP for PCI Express Root Port Base Address Register Decode Not Working Correctly	17-04-12	Version 11.0		http://www.altera.com/support/kdb/solutions/fb43785.html
PCI Express VHDL Example Design Simulation Fails	8-Feb-12	Version 11.1		http://www.altera.com/support/kdb/solutions/spr393995.html

Table 34–2. Hard IP for PCI Express Errata Knowledge Base Links (Part 3 of 3)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Gen2 Stratix V ES Hard IP for PCI Express IP Core Does Not Train with Gen3 Capable Root Port	6-Jan-12	Version 11.1		http://www.altera.com/support/kdb/solutions/spr393764.html
Stratix V Hard IP for PCI Express IP Core Does Not Perform Optional Address Translation Check	2-Dec-11	Version 11.0 SP1		http://www.altera.com/support/kdb/solutions/fb24784.html
Root Port Bus Functional Model (BFM) and Endpoint Design Example Not Available	9-Nov-11	Version 11.0 SP1		http://www.altera.com/support/kdb/solutions/spr380781.html
Stratix V Hard IP for PCI Express Root Port Bus and Device Number Restrictions	30-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr392894.html

35. Triple Speed Ethernet

Product Revision History

Table 35–1 shows the revision history for the Triple Speed Ethernet MegaCore function.

For more information about the new features, refer to the *Triple Speed Ethernet MegaCore Function User Guide*.

Table 35–1. Triple Speed Ethernet MegaCore Function Revision History

Version	Date	Description
12.1	June 2012	Preliminary support for Cyclone V devices.
11.1	November 2011	Preliminary support for Arria V devices.
11.0	May 2011	■ Final support for Cyclone IV GX, Cyclone IV E, Cyclone III LS, Arria II GZ, HardCopy III E and HardCopy IV E/GX devices.

Errata

For a recent list of errata for the Triple Speed Ethernet MegaCore function, refer to the AlteraKnowledge Base web page. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the Triple Speed Ethernet MegaCore function.

Table 35–2 lists the errata for the Triple Speed Ethernet MegaCore function, the relevant software releases, and links to the Knowledge Base.

Table 35–2. Triple Speed Ethernet MegaCore Function Errata Knowledge Base Links (Part 1 of 4)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
Recovered Clock Not Supported for Arria V GT Designs	06-Jul-12	12.0		http://www.altera.com/support/kdb/solutions/fb46847.html
Arria V and Arria V GT Designs Fail Hold Time Requirements in TimeQuest Timing Analyzer	06-Jul-12	12.0		http://www.altera.com/support/kdb/solutions/fb51702.html
Critical Warning for Designs with Reconfiguration Megafunction	06-Jul-12	12.0		http://www.altera.com/support/kdb/solutions/fb53896.html
Transmit Data Error in 1000BASE-X/SGMII PCS	02-Jul-12	11.1	11.1	http://www.altera.com/support/kdb/solutions/fb61021.html
MAC Function Stops Reading from Receive FIFO Buffer before Almost Empty Threshold is Reached	02-Jul-12	11.1	11.1	http://www.altera.com/support/kdb/solutions/fb61022.html

Table 35–2. Triple Speed Ethernet MegaCore Function Errata Knowledge Base Links (Part 2 of 4)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
XON Pause Frames are Sent when Receive FIFO Buffer is Congested	02-Jul-12	11.1	11.1.2	http://www.altera.com/support/kdb/solutions/fb61023.html
EtherStatsOversizePkts Statistic Counter Increase when MAC Function Receives VLAN or Stacked VLAN Tagged Frame	02-Jul-12	11.1	11.1.2	http://www.altera.com/support/kdb/solutions/fb61025.html
Incorrect Transceiver Receive Clock for 1000BASE-X/SGMII PCS in 1000BASE-X Mode	02-Jul-12	11.1	11.1.2	http://www.altera.com/support/kdb/solutions/fb61027.html
Jabbers and OversizePkts Counters Issues	02-Jul-12	11.1	11.1.2	http://www.altera.com/support/kdb/solutions/fb61028.html
Fragments and UndersizePkts Counters Issues	02-Jul-12	11.1	11.1.2	http://www.altera.com/support/kdb/solutions/fb61030.html
MAC Function Does Not Assert ff_rx_dsav Signal when 64-byte Frame is Received	02-Jul-12	11.1	11.1.2	http://www.altera.com/support/kdb/solutions/fb61031.html
rx_recovclkout Not Supported in Arria V GX	15-Feb-12	11.0		http://www.altera.com/support/kdb/solutions/spr393972.html
Intermittent Data Corruption	15-Feb-12	11.0		http://www.altera.com/support/kdb/solutions/spr393971.html
Unable to Bring-Up Individual Transceiver Channel	15-Feb-12	11.1		http://www.altera.com/support/kdb/solutions/spr393067.html
Extra Preamble on GMII Receive Interface Due to PPM Frequency Difference	15-Feb-12	11.0	11.1	http://www.altera.com/support/kdb/solutions/spr384491.html
Simulation Fails for Stratix V Designs Generated Using SOPC Builder	15-Nov-11	10.0		http://www.altera.com/support/kdb/solutions/spr392689.html
Auto-Negotiation Could Not Complete in 1000BASE-X PCS Function	15-Nov-11	10.0		http://www.altera.com/support/kdb/solutions/spr378244.html
Fitter Error for Cyclone IV GX Devices with 1000BASE-X/SGMII PCS Functions	15-Nov-11	10.1	11.0	http://www.altera.com/support/kdb/solutions/spr371799.html
Packet Loss in 8-bit Internal FIFO Buffer	15-Nov-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/spr3690530.html
Late Collision in Half-Duplex 10/100-Mbps Ethernet MAC	15-Nov-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/spr368541.html
Non-Compliant Implementation of aAlignmentError Statistics Counter	26-Sep-11	10.0		http://www.altera.com/support/kdb/solutions/spr272530.html
Timing Not Met in Cyclone III Devices	26-Sep-11	10.0		http://www.altera.com/support/kdb/solutions/spr302134.html
Serial Loopback is Enabled by Default in Cyclone IV GX Devices	26-Sep-11	10.0		http://www.altera.com/support/kdb/solutions/spr392706.html

Table 35–2. Triple Speed Ethernet MegaCore Function Errata Knowledge Base Links (Part 3 of 4)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
Transceiver Quad Sharing Failure	15-Nov-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/sp r369064.html
Corrupted Packets in 10/100-Mbps Designs with GXB Transceiver	26-Sep-11	10.0	10.1	http://www.altera.com/support/kdb/solutions/sp r392705.html
Half-Duplex Mode Post Collision Issues	15-Nov-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/sp r369063.html
Continuous Data Transmission from MAC Function	15-Nov-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/sp r369067.html
MII Local Loopback Failure	15-Nov-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/sp r369070.html
Unstable Designs with LVDS in Hardware	26-Sep-11	10.0		http://www.altera.com/support/kdb/solutions/sp r392707.html
PLL Sharing Problem for LVDS Channels	15-Nov-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/sp r369065.html
Critical Warning Message for HardCopy Devices	15-Nov-11	11.0		http://www.altera.com/support/kdb/solutions/sp r374163.html
Critical Warning Messages for 1000BASE-X/SGMII PCS Functions	15-Nov-11	11.0		http://www.altera.com/support/kdb/solutions/sp r392695.html
Critical Warning Messages When Local Loopback is Enabled	15-Nov-11	11.0		http://www.altera.com/support/kdb/solutions/sp r392696.html
Non-Compliant Implementation of Bit PAGE_RECEIVE in PCS Register	26-Sep-11	10.0		http://www.altera.com/support/kdb/solutions/sp r270637.html
Reset Synchronization Problem	15-Nov-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/sp r369069.html
Simulation Fails for HardCopy IV GX with GXB Transceiver	15-Nov-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/sp r374317.html
Speed Change Causes Corrupt Packet	15-Nov-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/sp r3690531.html
Statistics Counters Issues	15-Nov-11	10.0	11.0	http://www.altera.com/support/kdb/solutions/sp r369057.html
Unconstraint Clock in Stratix V Designs with GXB Transceiver and Transceiver Reconfiguration Controller Megafunction	15-Nov-11	11.0		http://www.altera.com/support/kdb/solutions/sp r392690.html
Timing Not Met in Stratix V Devices	15-Nov-11	11.0		http://www.altera.com/support/kdb/solutions/sp r392693.html
Hold Time Requirement Not Met in Stratix V Devices	15-Nov-11	11.1		http://www.altera.com/support/kdb/solutions/sp r389213.html
Warning Messages for Stratix V Designs	15-Nov-11	11.0		http://www.altera.com/support/kdb/solutions/sp r379766.html

Table 35–2. Triple Speed Ethernet MegaCore Function Errata Knowledge Base Links (Part 4 of 4)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
Critical Warning Message for Stratix V Devices	15-Nov-11	11.0		http://www.altera.com/support/kdb/solutions/spr392694.html
Compilation Targeting a Stratix V Device Fails	26-Sep-11	10.1	11.0	http://www.altera.com/support/kdb/solutions/spr3655401.html

36. Video and Image Processing Suite

Product Revision History

Table 36–1 shows the revision history of the Video and Image Processing Suite MegaCore functions.

For information about the new features, refer to the Video and Image Processing Suite User Guide.

Table 36–1. Video and Image Processing Suite Revision History

Version	Date	Description
12.0	July 2012	■ Added Avalon® Streaming (Avalon-ST) Video Monitor MegaCore Function. ■ Added Trace System MegaCore Function.
11.1	November 2011	Maintenance release.
11.0	May 2011	■ Added Deinterlacer II MegaCore function. ■ Added new polyphase calculation method for Scaler II MegaCore function. ■ Final support for Arria II GX, Arria II GZ, and Stratix V devices.

Errata

For the most recent list of errata for the Video and Image Processing Suite MegaCore functions, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the Video and Image Processing Suite MegaCore functions.

Table 36–2 lists the errata for the Video and Image Processing Suite MegaCore function, the relevant software releases, and links to the Knowledge Base.

Table 36–2. Video and Image Processing Suite MegaCore Function Errata Knowledge Base Links (Part 1 of 3)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
Scaler II Generates Incorrect Output When Receiving Empty Packets	21-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr354331.html
Clocked Video Output Incorrectly Aligns Start of Frame (vid_sof)	21-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr327890.html
Video and Image Processing Suite Fails to Launch in Windows	21-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr376112.html

Table 36–2. Video and Image Processing Suite MegaCore Function Errata Knowledge Base Links (Part 2 of 3)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
Scaler II Generates Incorrect Output When It Receives Elongated Control Packet	21-Nov-11	Version 10.0	Version 10.1	http://www.altera.com/support/kdb/solutions/spr375361.html
Incorrect Simulation Models Created for Deinterlacer and Frame Buffer	21-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr288288.html
Packets Sent to VIP Cores Must Have Non-Empty Payload	21-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr274423.html
Scalar Coefficients Preview Window Cannot be Closed	21-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr251844.html
Signed Vertical Coefficients and Unsigned Horizontal Coefficients (or Vice Versa) with Sum of Coefficients More Than 1 Cause Scaler II to Generate Incorrect Output	21-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr370402.html
Scaler II Generates Incorrect Output When Vertical Filter Taps is 3	21-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr370404.html
The 2D Median Filter Does Not Support 7×7 Filter Size	21-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr288376.html
Deinterlacer and Frame Buffer Connected to DDR3 May Not Work Properly	21-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr354512.html
Quartus II Compile Failure for VIP Clocked Video Output (CVO) Core due to Undeclared Variable	16-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr391280.html
Deinterlacer and Test Pattern Generator May Not Upgrade	21-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr298311.html
Compilation Fails on the Windows 7 or Vista Operating System	21-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr321624.html
RTL Simulation Reports Errors When Using Verilog HDL	21-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr289791.html
Scaler: Number of Colour Planes Incorrect	21-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr324689.html
Precision Must be Set When Using Lanczos Coefficients in Scaler	21-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr236867.html
Compilation Errors with the Frame Buffer	21-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr332336.html
SOPC Builder Avalon-ST Adapter Does Not Support Avalon-ST Video	21-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr273657.html
Frame Buffer and Deinterlacer are Missing Entry in .sdc File	21-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/spr323417.html

Table 36–2. Video and Image Processing Suite MegaCore Function Errata Knowledge Base Links (Part 3 of 3)

Issue	Last Modified Date	Version Found In	Version Fixed In	Knowledge Base Link
Cyclone II M4K Fails in Alpha Blending Mixer and Gamma Corrector	21-Nov-11	Version 10.0		http://www.altera.com/support/kdb/solutions/fb27180.html
High Number of Critical Warnings During Compilation for Deinterlacer II and Video Frame Buffer	21-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr375125.html
Scaler II Coefficients MIF for Simulation Missing in Qsys	21-Nov-11	Version 11.0		http://www.altera.com/support/kdb/solutions/spr374652.html

37. Viterbi Compiler

Revision History

Table 37–1 shows the revision history for the Viterbi Compiler.

For more information about the new features, refer to the *Viterbi Compiler User Guide*.

Table 37–1. Viterbi Compiler Revision History

Version	Date	Description
12.0	July 2011	Verified in the Quartus II software v12.0.
11.1	November 2011	Maintenance release.
11.0	May 2011	■ Final support for Arria II GX, Arria II GZ, Cyclone III LS, and Cyclone IV GX devices. ■ HardCopy Compilation support for HardCopy III, HardCopy IV E, and HardCopy IV GX devices.

Errata

For the most recent list of errata for the Viterbi Compiler, refer to the Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the Viterbi Compiler.

Product Revision History

Table 38–1 shows the revision history for the XAUI PHY IP core.

For more information about the new features, refer to the "*XAUI PHY IP Core*" chapter in the *Altera Transceiver PHY IP Core User Guide*.

Table 38–1. XAUI PHY Revision History

Version	Date	Description
12.0	June 2012	■ Added the following QSF settings to all transceiver PHY: ■ XCVR_TX_PRE_EMP_PRE_TAP_USER ■ XCVR_TX_PRE_EMP_2ND_POST_TAP_USER ■ Added 11 new settings for GT transceivers.
11.1	November 2011	Added **base data rate**, **lane rate**, **input clock frequency**, and **PLL type** parameters.
11.0	May 2011	Added support for DXAUI. Added support for Arria II GZ and HardCopy IV.

Errata

For a recent list of errata and affected versions of the XAUI PHY IP Core IP core, refer to the Altera Knowledge Base page of the Altera website. Also, you can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Not all issues affect all versions of the XAUI PHY IP Core.

Table 38–2 lists the errata for the XAUI PHY IP Core, the relevant software releases, and links to the Knowledge Base.

Table 38–2. XAUI PHY IP Core Errata Knowledge Base Links (Part 1 of 2)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
TimeQuest Timing Analyzer Might Improperly Report Setup Violations	8-Feb-12	Version 10.0	Version 10.0 SP1	http://www.altera.com/support/kdb/solutions/spr345689.html
Incorrect Addresses for XAUI Reset RX and TX Control and Status Registers	16-Sep-11	Version 10.0	Version 10.1	http://www.altera.com/support/kdb/solutions/spr350614.html

Table 38–2. XAUI PHY IP Core Errata Knowledge Base Links (Part 2 of 2)

Problem	Published Date	Version First Found	Version Fixed	Knowledge Base Link
Mixed Language Simulation Fails when Optimization Is On	16-Sep-11	Version 10.1	Version 11.1	http://www.altera.com/support/kdb/solutions/spr357410.html
Simulation of 10GBASE-R, Custom, Interlaken, Low Latency, PCI Express PIPE, and XAUI Transceiver PHY IP Cores Fails for Stratix V if You Use ModelSim With Mixed Languages	11-Nov-11	Version 10.1		http://www.altera.com/support/kdb/solutions/spr362110.html

This chapter provides additional information about the document and Altera.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."

Visual Cue	Meaning
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.